

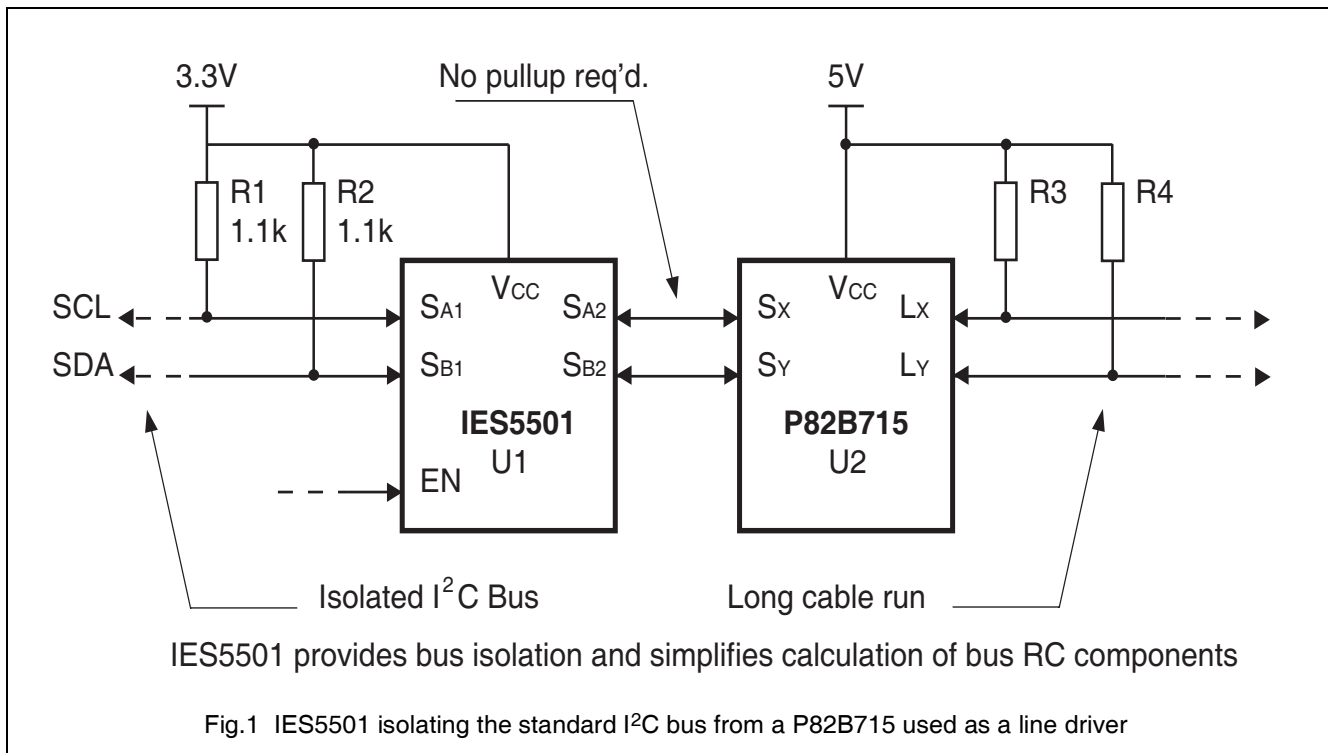
1 SUMMARY

The P82B715 Bus Extender can be quite complex to design into systems, especially in situations where the system structure may be changing due to adding and removing of components on the bus. Primarily this complexity is due to the fact that the P82B715 is non-isolating, and thus loads and pull-ups on both sides of the device must be considered together.

By adding an IES5501 to the Sx/Sy side of the P82B715, the bus calculations can be significantly simplified, and the I²C bus branch containing the P82B715 can be completely capacitively isolated from the remainder of the system.

2 FUNCTIONAL DESCRIPTION

2.1 Application Circuit



2.2 Description

Figure 1 shows how simply IES5501 interfaces with the Bus Extender P82B715 to enhance its functionality and simplify extended system design.

By providing a x10 current gain from its Sx/Sy side to its Lx/Ly side the P82B715 enables I²C devices, with 3mA static sink capability, to drive 30mA static loads on the bus at Lx/Ly. That in turn allows 10 times lower resistance pull-ups and 10 times greater bus capacitance on that bus at Lx/Ly so I²C systems with long runs of cable (at least 100 feet/30m) become possible. It is necessary to use at least two P82B715s, one at each end of the long cable, because normal I²C devices cannot be directly connected to the low impedance bus at Lx/Ly but only via another P82B715.

Because P82B715 has a finite gain (x10) the calculation of total system loading becomes quite tedious. For example, to calculate the system loading at the Sx/Sy interface in Figure 1 it is necessary to consider the loading on any remote I²C bus and then add 1/10 of the loading on the Lx/Ly bus. Especially in plug/play systems, where several modules may be connected to the low impedance bus, the system loading and choice of pull-ups can be complex.

Interfacing each local I²C bus to the Sx/Sy side of P82B715 via an IES5501 retains the key advantages of using P82B715 - rugged bipolar device, wide bus/Vcc supply range, and no changes to the bus logic levels (especially the lows). Interfacing with non-I²C parts (e.g micro-processors using TTL levels) is simple and the normal I²C noise margins are retained throughout the system.

The IES5501 adds the following system features/benefits:

- It provides true buffering (i.e. isolation) of the loading at its I/O ports
- It enables logic level shifting, simplifying the interfacing of each local I²C bus
- It provides the possibility to isolate the local bus by using its 'enable' control
- By adding some simple logic components it can provide isolation of the local I²C bus if bus lines are 'stuck low' e.g. if the P82B715 supply fails.

As explained in the P82B715 datasheet, using bus pull-ups at both Sx/Sy and Lx/Ly normally provides the best system performance and simplest system calculations.

That recommendation assumes that there will normally be significant loading on the Sx/Sy side of the P82B715. When directly interfaced only to IES5501, as in Figure 1, the IES5501 provides isolation of the loading at SCL/SDA and therefore minimal capacitive loading at Sx/Sy. With such small loading there, it is not as important to fit a local pull-up at Sx/Sy and no need to consider this Sx/Sy side loading in P82B715 system load calculations. In practice, with only the IES5501 at every Sx/Sy interface, the P82B715 system calculation simplifies to selection of the Lx/Ly bus pull-up to provide the desired rise-time for the capacitive loading on that bus alone.

2.3 Explanation

If no pull-up is used on the Sx side of P82B715 then that pin must be pulled high by the main pull-up on Lx. The current necessary to pull-up Sx then flows in the internal 30 ohm sense resistor and slows the turn off of the P82B715. If enough current flows at Sx, there can be enough drive to cause buffer action and any current

flowing out Sx will be multiplied x10. That larger current needs to be provided by the Lx pull-up.

That is why it is a good practice to use a local pull-up at Sx that causes a risetime at Sx to be at least as fast as the bus at Lx. In that case the buffer will turn off quickly and each side of the P82B715 can be calculated separately for purposes of determining the system risetime.

If the load at Sx is only 5-10pF, as in the case with only IES5501 connected, and the bus risetime is relatively slow as is usual when driving large capacitances or cables, then the load at Sx (say 10pF) simply adds to the load at Lx, which will usually already be of the order of several hundred pF, and so can be neglected in the calculations.

Even if there were 20 such modules connected, adding 200pF to the Lx bus loading, it still represents a minor loading, equivalent to 20pF on a standard I2C bus.

In such large systems, or systems with long cables, the capacitance alone is not necessarily the factor that dominates in determining the delays or bus risetime. Transmission line effects may need to be considered and even the simple limitation of the 30mA static sink current may preclude building systems with as many as 20xP82B715s. In those cases the true isolation of P82B96 is usually required but now the above solution, offering isolation without introducing any special logic level requirements, provides an alternative that can be particularly attractive in systems using TTL or SMBus logic levels.

The examples that follow illustrate how the slow, controlled, drive from the P82B715 is effective in minimising ringing when driving common types of cable that cannot be terminated in

their characteristic impedance (around 100 ohms).

When using this circuit arrangement, and especially when the IES5501 is used to achieve level-shifting to low voltage logic or TTL, it is necessary to ensure that severe ringing on long cables is not produced by compatible, but faster, drive ICs such as P82B96 or PCA9600. In systems where those devices may be interfaced to the same cable it is important to fit the

Schottky diode clamps, such as BAT54 variants, that are recommended when using those fast parts. They must be fitted across the Lx/Ly terminals of each P82B715.

2.4 Examples

To illustrate the performance, this combination of chips was used to drive 2m and 20m lengths of twisted pair communication cable. Two pairs from the four in Cat5e ethernet

communications cable were used. The other pairs had no signals on them.

2.4.1 20M CABLE

Fig.2 shows the test configuration for driving the cables. The I²C signals are input to the IES5501 at one end and recorded at various points as described.

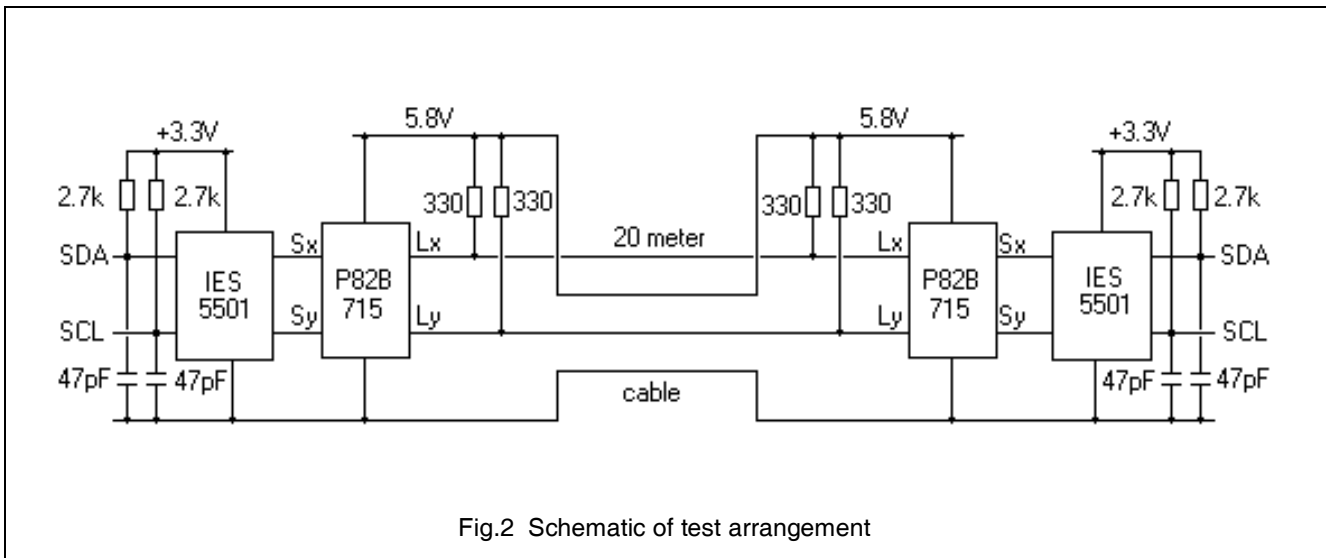


Fig.2 Schematic of test arrangement

The waveforms for a 20m cable are shown in Fig. 3.

Fig. 3 shows the SCL driving waveform and the 'received' waveform at the output side of the IES5501 at the receiving end.

The rise and fall times meet the 300ns Fast Mode requirement but the one-way propagation delay is about 400ns even when the drive is from a very fast LVC open drain gate so the total delay is likely to exceed 800ns, which is quite large when compared with the minimum 1300ns low period. It needs to be taken into account when selecting the system clock speed.

The overall dc offset of the bus low level, after passing through the 4 ICs, is still less than 500mV.

Figures 4 and 5 show the SCL waveform on the actual cable end as well as the IES5501 output SCL and SDA signals using a nominal 100kHz clock.

Note that the cable waveform drive in Fig. 4 has a relatively slow rise and fall time and this is mostly due to the controlled drive from P82B715 that ensures that there will be relatively little ringing and overshoot of the cable signals and contributes to maintaining good noise margins even when the IES5501 interface is 3.3V logic.

A pull-up could have been fitted at the Sx pins of P82B715 to improve the rising edge risetimes but the overall system timing gains will be small because the Sx only needs to rise to 1V to cause the IES5501 to release its output (2).

Fig.5 shows in more detail the SCL signals at the send and receive ends of the cable. On the falling edge there is some ringing at the receive end, but not below the allowed rating of -0.5V. For practical purposes, and except for maybe 70mV of dc offset, the signals at the Sx and Lx pins of the same P82B715 are always essentially identical.

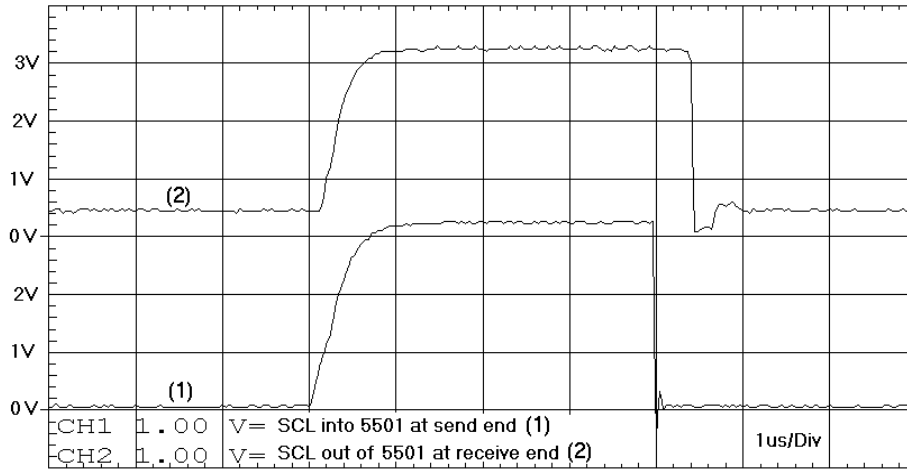


Fig.3 Sent and received signals for 20m cable

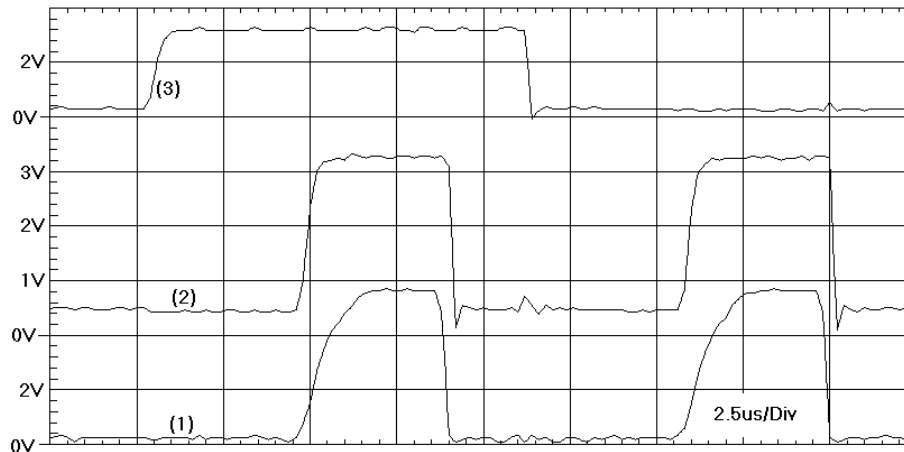
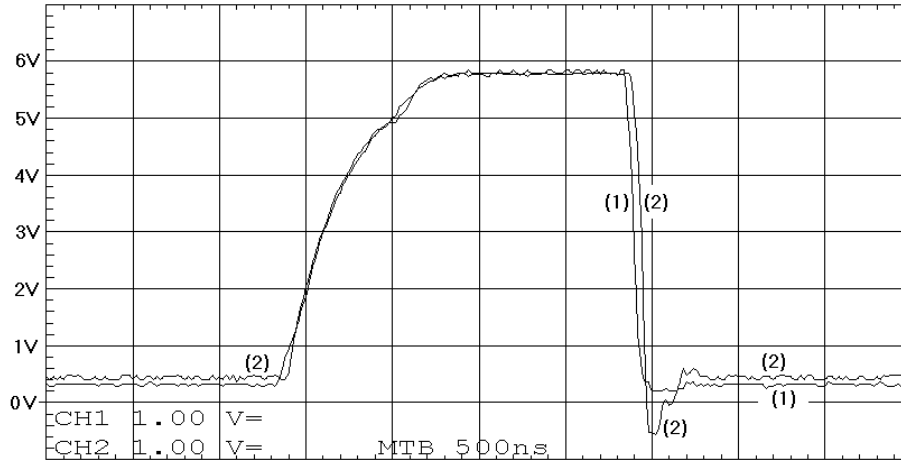


Fig.4 Waveforms on 20m cable



(1) SCL signal output at Lx by the driving P82B715
 (2) SCL signal output at Sx by the receiving P82B715

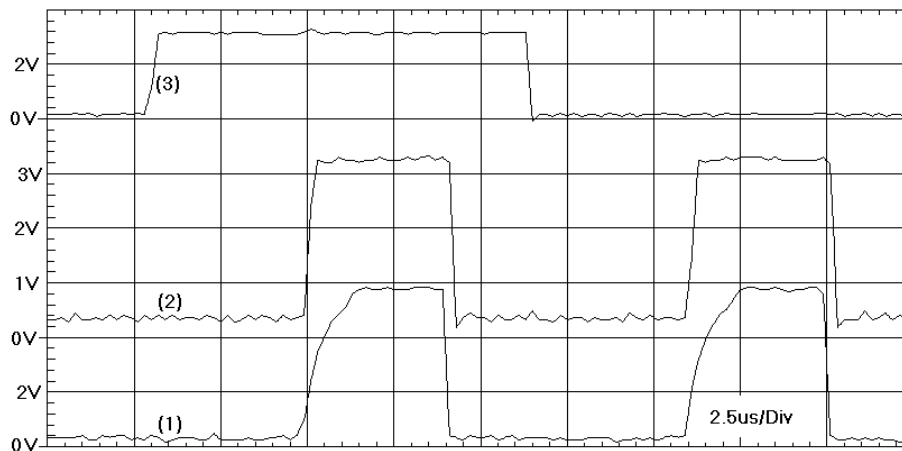
Fig.5 SCL send and receive waveforms measured on the cable

2.4.2 2M CABLE

Apart from the cable length, the test arrangement is the same as for the 20m cable.

Fig. 6 shows the signals for a short length of cable. Note that in this case the receiving end waveform after the P82B715 is shown to illustrate that ringing is smaller, and in this case

there is no ringing, for shorter cable lengths.



(1) SCL at receiving end of the cable output by P82B715 at Sx
 (2) SCL waveform output by IES5501 at receiving end of cable
 (3) SDA signal output by IES5501 at receiving end of cable.

Fig.6 Waveforms on 2m cable for nominal 100kHz clock

2.4.3 THE EFFECTS OF LOGIC LEVEL SHIFTING

In the examples above, the logic level shifting ability of IES5501 has been demonstrated by selecting a 3.3V supply for that chip while the P82B715 and the cable use 5.8V signals.

The use of a 3.3V supply on the IES5501 means compliant 3.3V logic switching levels at its I/Os that may be considered ideal for interfacing with 3.3V I²C parts.

The switching level for the cable signal is then also set at approximately 1V and that reduces the noise margins for the logic 'low' on the cable bus. That noise margin becomes approximately (1V- bus low voltage).

In the examples above the simulated driving I²C device has a Vol of just 50mV.

After the offsets of the low signal passing through the buffers is added, the dc component of the low level input to the receiving IES5501 at the other end of the cable is around 450mV. That means the actual noise margin is (1V - 0.45V) = 0.55V.

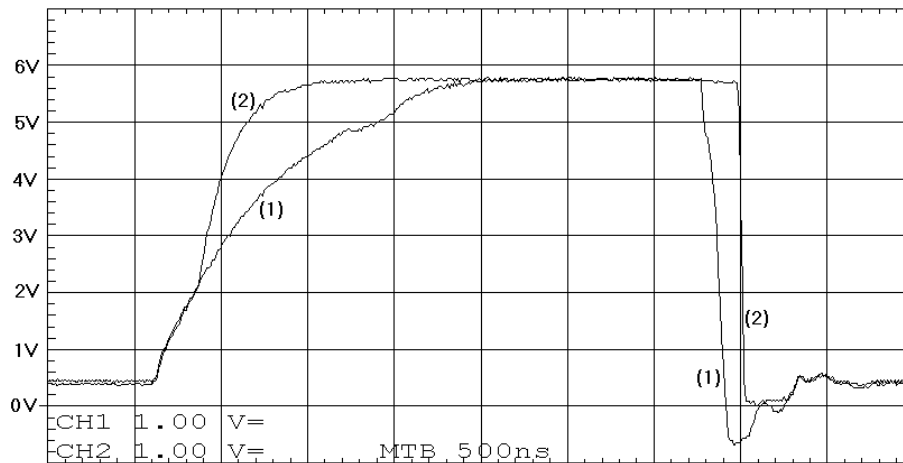
That is adequate for operation in environments with relatively low levels of interfering noise or differences in the ground potential level at the ends of the cable but clearly the tolerance to noise is being limited by the connected 3.3V I²C devices.

If the supply voltage to the connected devices, and the IES5501, is increased to the cable supply of 5.8V

then the logic switching level will be increased to 1.9V and the system noise margin will be increased by a substantial 0.9V. Selecting a more usual nominal 5V supply also provides a worthwhile improvement.

Fig. 7 shows the waveforms for a 20m cable with the receiving IES5501 supply connected to the P82B715 supply. The arrangement otherwise remains the same as in Fig. 2.

The point on the rising edge in Fig.7 where the output (2) is released happens after the switching threshold at approximately 1.9V is crossed and after the internal IES5501 propagation delay of about 50-100ns. Below that 1.9V switching threshold the output (2) simply follows the input (1).



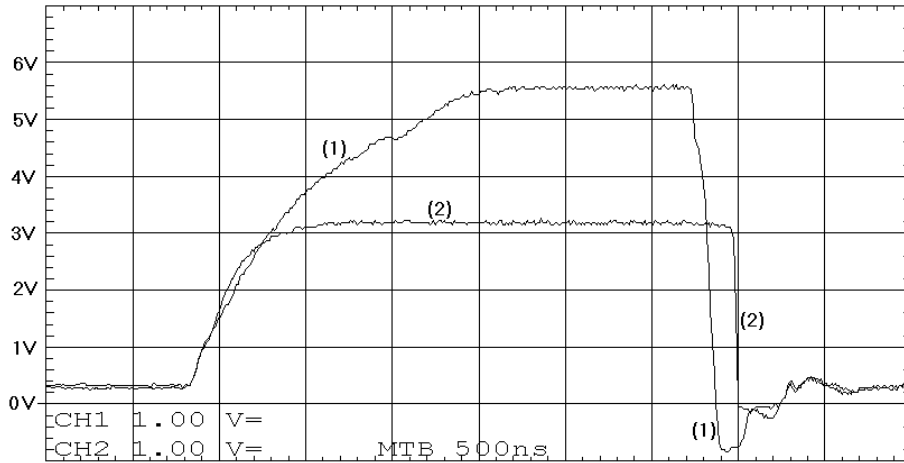
(1) SCL signal output by the P82B715 at the receiving end
 (2) SCL signal output by the IES5501 at the receiving end

Fig.7 Receiving IES5501 supply increased to 5.8V. 20m cable.

Two points to note when using the higher supply voltage are a) there is a longer propagation delay because the output follows the slowly rising cable waveform to a higher level and b) only noise on the cable signal that causes the signal level to exceed 1.9V can cause a 'glitch' to high on the output (2).

The corresponding waveforms for 3.3V supply on the receiving IES5501 are shown in Fig. 8. The typical (one way) propagation delay in Fig.7, compared with Fig. 8, is increased by only 150ns but there has been a useful increase in noise margin.

The increased propagation delay could, of course, be reduced by adding pull-ups to the 5.8V supply at the Sx/Sy pins of the P82B715. (But adding those pull-ups will hardly affect the delays when the supply is 3.3V)



(1) SCL signal output by the P82B715 at the receiving end
 (2) SCL signal output by the IES5501 at the receiving end

Fig.8 Receiving IES5501 supply is 3.3V. 20m cable.

3 DOCUMENT HISTORY

REVISION	DATE	DESCRIPTION
1.0	20061128	First released version
1.1	20070612	Added Sections 2.3 & 2.4
1.2	20070817	Typographical errors fixed. Added Figure 8

4 DEFINITIONS

Data sheet status	
Engineering sample information	This contains draft information describing an engineering sample provided to demonstrate possible function and feasibility. Engineering samples have no guarantee that they will perform as described in all details.
Objective specification	This data sheet contains target or goal specifications for product development. Engineering samples have no guarantee that they will function as described in all details.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later. Products to this data may not yet have been fully tested, and their performance fully documented.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

5 COMPANY INFORMATION

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