



## The precise logic switching voltage levels of IES5501 allow simple interfacing from 1.5V to 3.3V/ 5V levels

**Keywords:** Bus Buffer, I<sup>2</sup>C, IES5501, low voltage interfacing, offset voltage, noise margin

**Summary:** Bi-directional bus buffers don't receive information to set the data direction flow. To ensure latching doesn't occur the output voltage on the data lines must be larger than the input voltage. For a Fast Mode I<sup>2</sup>C system to comply with the specification, the bus low-level voltage must be  $<0.25V_{cc}$ . To meet this requirement, buffers designed with special output levels generally have output levels in the range of 0.5 to 1V and are therefore forced to use non-compliant input levels set below that range. Typical values are around 0.4V meaning their noise margin at that interface is very small. The solution is to use an I<sup>2</sup>C compliant buffer such as IES5501 that only adds a typical offset voltage of 60mV to the input giving the system more noise margin.

In this example the supply voltage for the IES5501 is selected as 2.7 – 3V and that determines the logic switching levels on all its I/Os. This supply may be derived by regulation, or possibly just by a simple diode drop from a 3.3V supply.

The typical logic switching level is  $0.33V_{cc}$  therefore, in this example is 0.9 – 0.99V. That is compatible with both the very low voltage logic and also with 3.3 – 5V logic.

The IES5501 logic 'low' requirement (ie worst case maximum level) will be  $0.3V_{cc}$  or 0.81 – 0.9V. While that is only 'compliant' with the worst case limits for I<sup>2</sup>C logic system voltages above 2.7V or the TTL logic levels used by derivative buses such as SMBus<sup>TM</sup>; in practice it will be compatible with even 5V I<sup>2</sup>C logic devices because they are required to produce a  $V_{ol} = 0.4V$  max.

Of course the noise margins on the 5V bus side are being compromised because they are reduced to the worst case

noise margins of the IES5501 when operating on its lowest supply (2.7V) but the worst case noise margin remains 0.41V and that is more than adequate in most practical applications where the parts are all mounted on the same printed circuit board.

The typical noise margin, at around 0.75V is quite large. To fully appreciate the logic levels and noise margins it is worth considering the typical levels that will be found in this system.

### 1. Logic low levels.

The 1.5V logic device must produce a  $V_{ol} < 0.4V$  and in practice will produce levels below half that level i.e. below 0.2V.

The IES5501 switching level is  $0.33V_{cc}$  so the noise margin on that low is at least  $(0.9 - 0.2) = 0.7V$ . The level delivered to the 5V devices on the other side of IES5501 will typically be 50mV higher or around

## DI003: Simple interfacing to very low voltage (1.5V) I<sup>2</sup>C logic levels

0.25V. The switching level of 5V I<sup>2</sup>C devices is nominally 2.5V or for TTL devices 1.4V, so in either case there is a good safety margin.

When the 5V logic device generates a low it is again required to be less than 0.4V and typically will be <0.2V. That is delivered by the IES5501 to the 1.5V logic device with just 50mV offset, so as typically 0.25V, max 0.45V.

The typical switching level of the 1.5V logic is 0.75V, so here the smallest (worst case) system safety (noise) margin ( $0.3V \times 1.5V - 0.45V = 0$ ) is 0V but the typical remains greater than the very reasonable ( $0.75V - 0.25V$ )  $\geq 0.5V$  and in practice there will be no problems with the operation.

### 2. Logic high levels.

Noise margins when the bus is high remain the usual normal and worst case ones in every case because IES5501 fully releases its buses and they are pulled up to their nominal bus supply voltage.

The capacitors marked 'C' on the figure are shown as a 'good design practice' for suppressing any high frequency ripple that is sometimes observed when wiring is not optimised for the 1MHz capable buffer. Typical values are 33-100pF. Supply bypassing is not shown but good practice would be to fit 10nF-100nF ceramic capacitors on all rails.

(Note: The IES5501 datasheet shows 1.8V as the lowest bus voltage. That value provides a larger noise margin and allows a wider allowable supply voltage range than quoted in this more specific application example. The intention here is to show how even 1.5V can be possible if other design compromises are acceptable.)

### Parts Ordering Information

Part Number	Package	Package Type
IES5501T	SO8	Tube
IES5501D	MSOP8	Tube
IES5501TR	SO8	Tape and Reel
IES5501DR	MSOP8	Tape and Reel

### Other Hendon Semiconductors related parts

Part Number	Description
IES5502	Fast dual bi-directional bus buffer with hot insertion logic
IES5505	Simple two wire bus buffer
IES5515	Simple two wire bus buffer

Designing an I<sup>2</sup>C system? Email the bus buffer experts at [hendon.info@hendonsemiconductors.com](mailto:hendon.info@hendonsemiconductors.com) for suggestions to optimize your system. For more information please visit [www.bus-buffer.com](http://www.bus-buffer.com)

### Contact Hendon Semiconductors

1 Butler Drive, Hendon SA 5014, AUSTRALIA  
Tel: +61 (8) 8348-5200 | Fax: +61 (8) 8243 1048  
Email: [hendon.info@hendonsemiconductors.com](mailto:hendon.info@hendonsemiconductors.com)

