



Low cost external circuits with IES5501 can provide a 'bus release' when required.

Keywords: Bus Buffer, I²C, IES5501, bus stuck low

Summary: When the SDA line is stuck at low level for longer than expected times, some systems require the disconnection of that particular section of the bus. The IES5501 can be connected to the Master in such a way that when a section of bus is stuck low, the Master can force an enabling of the buffer.

Some systems require the disconnection of sections of a bus system if the bus lines are stuck at the low level for longer than the expected normal times.

Since most slaves do not have any capability to drive the SCL bus low, normally only the SDA line can be 'stuck'. In that case the SCL bus could be directly connected (ie not through the buffer) so that after the Master finds any Slave is not responding it can attempt stuck bus recovery routines and if these are successful the buffer will re-enable the SDA connection as soon as SDA becomes free and goes high.

It is also possible to connect the IES5501 Enable pin via a diode to a port on the Master so that the Master can override this automatic disconnection and force an enabling of the buffer if required.

The IES5501 buffer has an internal pull-down current sink (nominal 2µA) on its Enable input pin. This can be

used to provide a disconnection of one side of the buffer if one of the I²C bus lines stay low for longer than a designed time period and to create a simple timer using an external capacitor.

If the Enable input is fitted with a storage capacitor and held high using the high gain transistor as shown then when the SDA bus goes low, the Enable pin will start to discharge the storage capacitor. If the voltage on the enable pin reaches 1V the IES5501 will be disabled and the 'stuck' SDA bus will be isolated from the rest of the bus system on the 'input' side of the buffer.

The transistor can be any NPN high gain small signal or switching transistor similar to the one shown provided its reverse emitter-base voltage rating is equal to the Vcc2 supply, or at least 5V if Vcc2 is at the maximum allowed 5.5V.

DI005: Releasing a 'Bus Stuck Low' section of an I²C systems

The capacitor will be discharged according to the formula

$CV=it$ where

- C = capacitance,
- V = change in voltage,
- i = internal sink current of the IES5501 (nominal 2 μ A, 3 μ A max) and
- t = time to change by the voltage V.

A typical time used for disconnection is 30ms and is generally is in the range 10-50ms. Using a timing capacitor of around 33nF as shown will provide a nominal time period of 16.5ms per volt of discharge.

For a 3.3V bus system, with the bus lines high, the Enable will be held at approximately 0.5V below V_{cc2}, because the voltage drop across the emitter-base at 2 μ A will be quite small. When SDA goes low the capacitor starts to discharge towards the 1V disable level and the typical time to decrease (3.3V – 0.5V) down to 1V, for a change of 1.8V, is about 30ms for the 33nF capacitor shown.

One typical stuck bus recovery routine is to generate 9 cycles of SCL, with SDA not driven, then try to send Start, Stop and one cycle of SCL. Then try to issue a sequence of Start, Stop, Start, Stop and then a Start followed by the slave address.

Part Ordering Information

Part Number	Package	Package Type
IES5501T	SO8	Tube
IES5501D	MSOP8	Tube
IES5501TR	SO8	Tape and Reel
IES5501DR	MSOP8	Tape and Reel

Other Hendon Semiconductors related parts

Part Number	Description
IES5502	Fast dual bi-directional bus buffer with hot insertion logic
IES5505	Simple two wire bus buffer
IES5515	Simple two wire bus buffer

Designing an I²C system? Email the bus buffer experts at hendon.info@hendonsemiconductors.com for suggestions to optimize your system. For more information please visit www.bus-buffer.com

Contact Hendon Semiconductors

1 Butler Drive, Hendon SA 5014, AUSTRALIA
Tel: +61 (8) 8348-5200 | Fax: +61 (8) 8243 1048
Email: hendon.info@hendonsemiconductors.com

