



Keywords: Bus Buffer, I²C, IES5501, AdvancedTCA, Shelf manager, IPMB, Fast mode, logic switching levels, compliant logic levels

Summary: Shelf Manager Controllers for IPMB systems 'should' have I²C compliant switching levels and require 'some active circuitry' to achieve the specified bus rise time into a specified load capacitance. Because IES5501 have compliant switching levels, addition of a simple active circuit to speed up the bus rising edges and provision of the passive bus pull up provides a complete low cost solution.

The AdvancedTCA specifications have always required that the IPMB and connected devices should be Fast Mode I²C compliant. Compliance requires that the bus logic switching levels meet the I²C specified 30%V_{cc} and 70%V_{cc} worst case Low and High switching levels, and that the bus lines must be free to be pulled up if the 3.3V supply fails. For the nominal 3.3V IPMB that means the compliant logic low level must include all voltages up to 30% x 3.3V or 0.99V.

The IPMB specifications depart from the conventional Fast mode I²C specification in these important requirements:

1. The bus pull-up resistor must be exactly 2.7k. (The I²C specifications allow down to slightly less than 1k)
2. The maximum bus capacitance is increased to 690pF (I²C limit 400pF)
3. The bus rise time is 900ns (Fast Mode I²C requires 300ns)

The specification of a larger minimum pull-up was necessary to keep the input-output offset of the buffer originally used down to a workable value (around 0.1V typical) because those early buffers also require a maximum input low level of typically 0.5V – equal to the

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allowed IPMB maximum level – leaving zero safety margin.

Today the IES5501 offers compliant switching levels (0.3V_{cc} or 0.99V, well above that problem 0.5V level, and also has smaller offsets. IES5501 offset is specified at 0.06V maximum (0.03V typ.) at the reduced IPMB currents.

It can be shown that the IPMB 2.7K pull-up requires just 0.63mA additional pull-up current to meet the 900ns requirement on bus rising edges. That can be provided by the low cost discrete components shown in the schematic above.

This can be assembled with components on only one side of a PCB area about 0.8 cm², or purchased pre-assembled as HM234 suitable for surface mounting onto an existing PCB area 0.95cm x 0.95cm. It will reject spurious noise steps up to at least 0.5V high yet operate as required only on normally rising bus edges. The DTC124E logic transistor ensures Fast Mode compliance with the requirement that the Accelerator not load the bus lines if the 3.3V supply fails.

More details and bus waveforms can be found in [AN101 Discrete Rise Rate Accelerators with IES5501 in Bused AdvancedTCA system](#).

The active shelf manager (in simple bused configurations) is also required to provide the passive 2.7K bus pull-up. On the schematic this is shown with an option to disconnect these resistors when this controller is not the active shelf manager. Normally the processor controls a FET analog switch (with no diodes to its V_{cc}) to provide this feature in a compliant way.

For alternative solutions and other IPMB applications see other application sheets and [AN103 Use of IES5501 in AdvancedTCA applications](#).

Part Ordering Information

Part Number	Package	Package Type
IES5501T	SO8	Tube
IES5501D	MSOP8	Tube
IES5501TR	SO8	Tape and Reel
IES5501DR	MSOP8	Tape and Reel

* HM234 Discrete rise rate accelerator demo kit can be requested free from Hendon Semiconductors.

Other Hendon Semiconductors related parts

Part Number	Description
IES5502	Fast dual bi-directional bus buffer with hot insertion logic
IES5505	Simple two wire bus buffer
IES5515	Simple two wire bus buffer

Designing an I²C system? Email the bus buffer experts at hendon.info@hendonsemiconductors.com for suggestions to optimize your system. For more information please visit www.bus-buffer.com

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