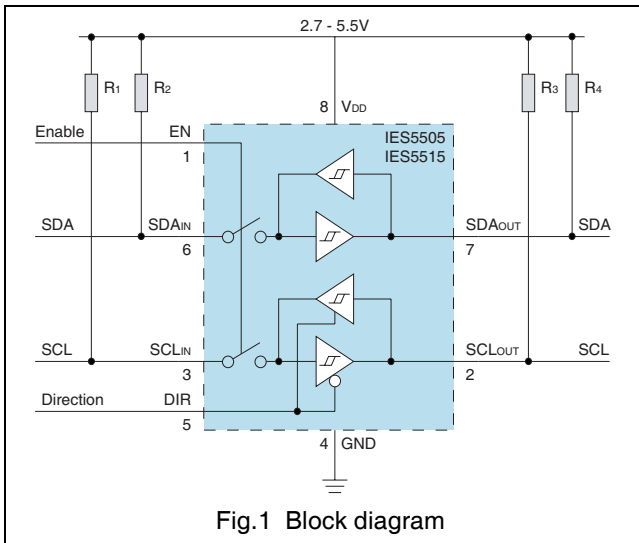


### 1 FEATURES

- Simple impedance isolating buffer for 2-wire buses
- 30mA (IES5515) or 4mA (IES5505) maximum static pull-down capability supports a wide range of bus standards
- Works with I<sup>2</sup>C<sup>(1)</sup> bus Standard mode, Fast mode, Fast mode plus Fm+ (IES5515), SMBus (standard and high power mode), and PMbus
- Fast switching times allow operation in excess of 1MHz
- Enable allows bus segments to be disconnected
- Hysteresis on inputs provides noise immunity
- Operating voltages from 2.7 V to 5.5 V
- Very low supply current
- Uncomplicated characteristics suitable for quick implementation in most common 2-wire bus applications

### 2 BLOCK DIAGRAM



### 3 GENERAL DESCRIPTION

The IES5505 and IES5515 are monolithic CMOS integrated circuits for bus buffering in applications including I<sup>2</sup>C, SMBus, DDC, PMbus, and other systems based on similar principles.

The buffer extends the bus load limit by buffering both the SCL and SDA lines, allowing the maximum permissible bus capacitance on both sides of the buffer.

The IES5505/15 includes a uni-directional buffer for the clock signal, and a bi-directional buffer for the data signal. Slave devices which employ clock stretching are therefore not supported.

In its most basic implementation, the buffer will allow an extended number of Slave devices to be attached to one (or more) Master devices. In this case, all Master devices would be positioned on the Sxx<sub>IN</sub> side of the IES5505/15.

The Direction pin further enhances this function by allowing the uni-directional clock signal to be reversed, thus allowing Master devices on both sides of the buffer.

The Enable function allows sections of the bus to be isolated. Individual parts of the system can be brought on-line successively. This means a controlled start-up using a diverse range of components, operating speeds and loads is easily achieved.

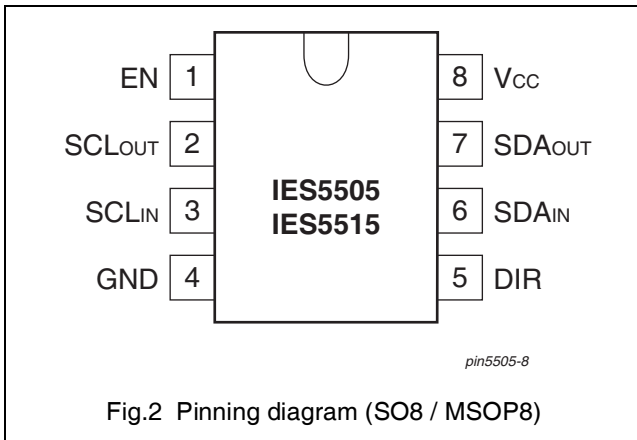
### 4 APPLICATIONS

- Electronic Signs & Displays
- Lighting Control (incl. Architectural & Stage lighting)
- Game Consoles / Boxes
- Gaming Machine Networks
- Building Automation
- TV / Projector / Monitor interconnection (DDC)
- Power Management Systems
- Desktop and Portable Computers
- Security Systems
- Interfacing standard 3mA I<sup>2</sup>C parts to a 30mA Fm+ bus

(1) I<sup>2</sup>C-bus is a trademark of NXP B.V.

### 5 PINNING INFORMATION

#### 5.1 Pinning layout



### 6 FUNCTIONAL DESCRIPTION

#### 6.1 V<sub>DD</sub>, GND - DC supply pins

The power supply voltage for the IES5505/15 may be any voltage in the range 2.7 V to 5.5 V. The IC supply must be common with the supply for the bus. Hysteresis on the ports is a percentage of the IC's power supply, hence noise margin considerations should be taken into account when selecting an operating voltage.

#### 6.2 SCL<sub>IN</sub>, SCL<sub>OUT</sub> - Clock Signal inputs/outputs

The clock signal buffer is uni-directional, though the direction may be reversed under control of the Direction pin. In normal bus operations, for example the I<sup>2</sup>C bus, the Master device generates a uni-directional clock signal to the slave. For lowest cost the IES5505/15 combines uni-directional buffering of the clock signal with a bi-directional buffer for the data signal. Clock stretching is therefore not supported and Slave devices that may require clock stretching must be accommodated by the Master adopting an appropriate clocking when communicating with them. The buffer includes hysteresis to ensure clean switching signals are output, especially with slow rise times on high capacitively loaded buses.

#### 6.3 SDA<sub>IN</sub>, SDA<sub>OUT</sub> - Data Signal inputs/outputs

The data signal buffer is bi-directional. The port (SDA<sub>IN</sub>, SDA<sub>OUT</sub>) which first falls below the "lock-out voltage" V<sub>LK</sub>, will take control of the buffer direction and "lock out" signals coming from the opposite side. As the "input" signal continues to fall, it will then drive the "output" side low. Again, hysteresis is applied to the buffer to minimise the effects of noise.

#### 5.2 Pin description

SYMBOL	PIN	DESCRIPTION
EN	1	Enable
SCL <sub>OUT</sub>	2	Clock Buffer "Slave Side"
SCL <sub>IN</sub>	3	Clock Buffer "Master Side"
GND	4	Supply Ground
DIR	5	Clock Direction
SDA <sub>IN</sub>	6	Data Buffer "Master Side"
SDA <sub>OUT</sub>	7	Data Buffer "Slave Side"
V <sub>DD</sub>	8	Positive supply

At some points during the communication, the data direction will reverse - for example, when the Slave transmits an acknowledge (ACK), or responds with its register contents. During these times, the controlling "input" side will have to rise back above the lock-out voltage (V<sub>LK</sub>) before it releases the "lock", which then allows the "output" side to gain control, and pull (what was) the "input" side low again. This will cause a "pulse" on the "input" side, which can be quite large in high capacitance buses. However, this pulse will not interfere with the actual data transmission, as it should not occur during times of clock line transition (during normal I<sup>2</sup>C and SMBus protocols), and thus data signal set-up time requirements are still met.





#### 6.4 Enable (EN) - Activate Buffer Operations

The active-high Enable input can be used to disable the buffer, for the purpose of isolating sections of the bus. The IC should only be disabled when the bus is idle. This prevents truncation of commands which may confuse other devices on the bus. Enable may also be used to progressively activate sections of the bus during system start-up. Bus sections slow to respond on power-up can be kept isolated from the main system to avoid interference and collisions.

#### 6.5 Direction (DIR) - Clock Buffer Direction Control

The Direction input is used to change the signal direction of the SCL ports. When the Direction pin is logic "low", the clock signal input is SCL<sub>IN</sub> and the buffered output is SCL<sub>OUT</sub>. When the Direction pin is logic "high", the clock signal input is SCL<sub>OUT</sub> and the buffered output is SCL<sub>IN</sub>.

### 7 ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	NAME	DESCRIPTION	VERSION	ROHS
IES5505 T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1	Yes 
IES5505 D	MSOP-8L	micro small outline package; 8 leads; body width 3.0 mm	SOT505-1	Yes 
IES5515 T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1	Yes 
IES5515 D	MSOP-8L	micro small outline package; 8 leads; body width 3.0 mm	SOT505-1	Yes 

Other package options are available - contact Hendon Semiconductors for details. For more information on packages, please refer to the document "Integrated Circuit Packaging and Soldering Information" on the Hendon Semiconductors web site.

### 8 ESD CAUTION

Electrostatic Discharge (ESD) sensitive device. ESD can cause permanent damage or degradation in the performance of this device. This device contains ESD protection structures aimed at minimising the impact of ESD. However, it is the users responsibility to ensure that proper ESD precautions are observed during the handling, placement and operation of this device.



### 9 DOCUMENT HISTORY

REVISION	DATE	DESCRIPTION
0.4	20071015	Company Name Change
0.5	20080107	Merge IES5505 & IES5515 datasheets
0.6	20080131	Product Brief
0.7	20080226	Preliminary Status

**10 DEFINITIONS**

<b>Data sheet status</b>	
Engineering sample information	This contains draft information describing an engineering sample provided to demonstrate possible function and feasibility. Engineering samples have no guarantee that they will perform as described in all details.
Objective specification	This data sheet contains target or goal specifications for product development. Engineering samples have no guarantee that they will function as described in all details.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later. Products to this data may not yet have been fully tested, and their performance fully documented.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

**11 COMPANY INFORMATION**

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