

### 1 FEATURES

- 8 individually selectable open drain output ports
- 65mA static sink capability on all output ports
- Ports may be paralleled for up to 500mA drive
- Ideal for simple LED or general purpose output drive
- Fast Mode Plus (30mA, 4000pF) 2-wire bus capability.
- Works with I<sup>2</sup>C-bus<sup>(1)</sup> (Standard, Fast Mode, and FM+), SMBus (standard and high power mode), and PMbus
- Fast switching times allow operation in excess of 1MHz
- Operating voltages from 2.7 V to 5.5 V
- Uncomplicated characteristics suitable for quick implementation in most common 2-wire bus applications

### 2 APPLICATIONS

- LED and 7-segment displays;
- Simple high-power (500mA) LED dimming;
- General Purpose Output;
- Instrumentation indicators;

(1) I<sup>2</sup>C-bus is a trademark of NXP B.V.

### 3 GENERAL DESCRIPTION

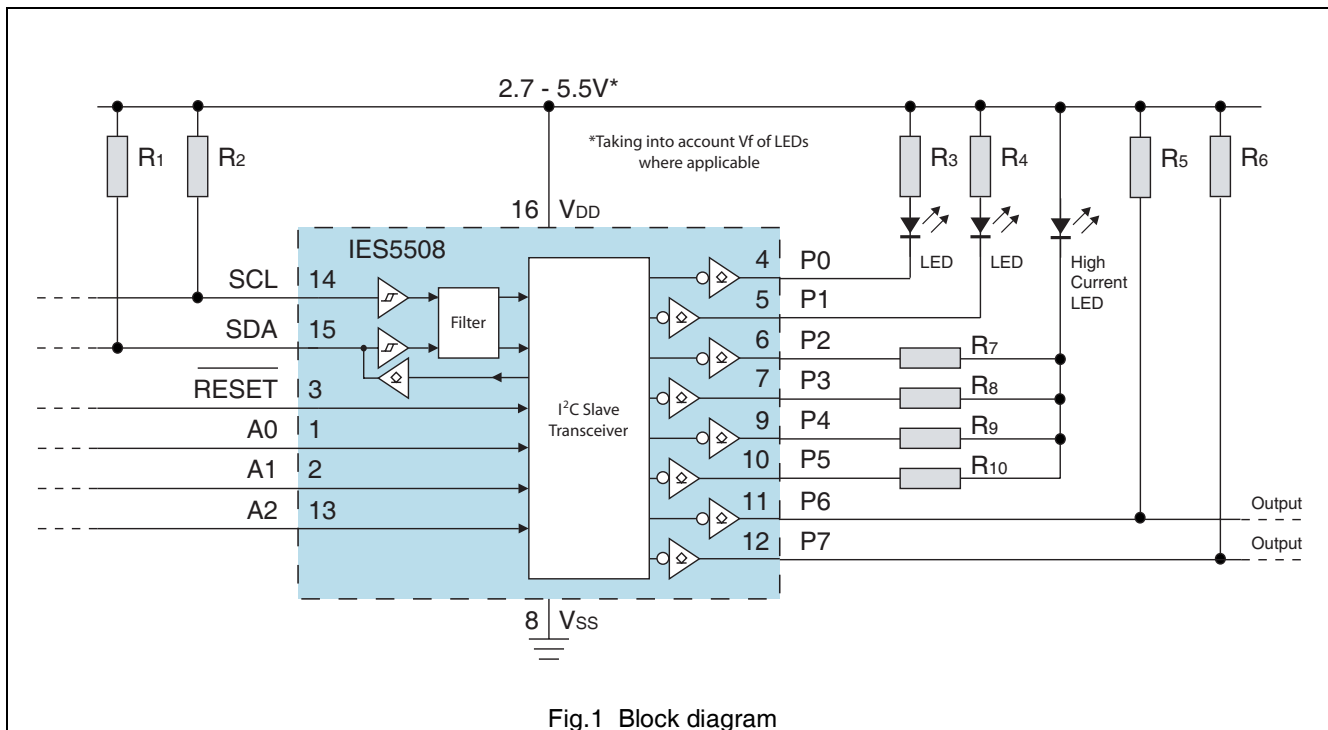
The IES5508 is a monolithic CMOS integrated circuit for general purpose output drive configurable from a 2-wire bus interface (including I<sup>2</sup>C-bus, SMBus, PMbus, and other systems based on similar principles). Output ports have a 65mA sink capability, making them ideal for driving LEDs.

The state of the outputs is determined by a programmable 8-bit register which can be read and written via signals from the 2-wire bus (e.g. I<sup>2</sup>C or similar).

The 2-wire bus interface also has 30mA Fast Mode Plus (FM+) capability, and consequently can be run in excess of 1MHz or up to 4000pF capacitance. As such, the IES5508 can be connected to other 2-wire devices across long cable connections.

It interfaces excellently with the IES5515 (2-wire buffer) and IES5507 (2-wire 4-way bus multiplexer) devices to provide the high-speed or high-capacitance drive. Together this family provides a simple way of producing (for example) large scale LED displays.

### 4 BLOCK DIAGRAM

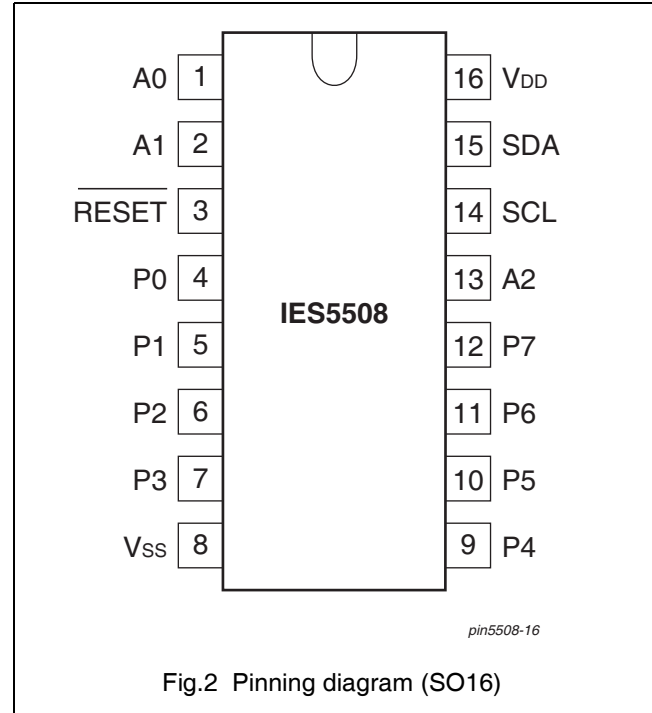


### 5 PINNING INFORMATION

#### 5.1 Pin description

SYMBOL	PIN	DESCRIPTION
A0	1	Address Input 0
A1	2	Address Input 1
$\overline{\text{RESET}}$	3	Active Low Reset Input
P0	4	Output Port 0
P1	5	Output Port 1
P2	6	Output Port 2
P3	7	Output Port 3
V <sub>SS</sub>	8	Negative supply (ground)
P4	9	Output Port 4
P5	10	Output Port 5
P6	11	Output Port 6
P7	12	Output Port 7
A2	13	Address Input 2
SCL	14	Serial Clock Line
SDA	15	Serial Data Line
V <sub>DD</sub>	16	Positive supply

#### 5.2 Pinning layout



### 6 FUNCTIONAL DESCRIPTION

#### 6.1 V<sub>DD</sub>, V<sub>SS</sub> - DC supply pins

The power supply voltage for the IES5508 may be any voltage in the range 2.7 V to 5.5 V, though in LED driving applications, the forward voltage of the LED and the V<sub>OL</sub> of the IES5508 must be taken into account.

#### 6.2 SCL, SDA - 2-Wire Bus Interface

The state of the output ports is determined by the control register, which is set and read via a 2-wire bus interface using I<sup>2</sup>C style signalling. The interface is Fast Mode Plus (FM+) I<sup>2</sup>C compatible, though the ports contain ESD protection diodes to the positive and negative supplies. Consequently V<sub>BUS</sub> (max. voltage at SCL & SDA) must remain within the V<sub>DD</sub> and V<sub>SS</sub> supply levels.

#### 6.3 P0 to P7 - Output Ports

There are 8 open-drain output ports whose state is determined by the control register. Programming a '1' or HIGH to the relevant register bit will turn on corresponding

the port, resulting at a LOW or '0' at the port. In the case of LED driving, this would result in the LED turning ON.

Programming a '0' or LOW in the register turns off the open-drain port, placing it in a high-impedance mode.

Ports also are protected by ESD diodes to the supplies, and cannot be driven above or below the V<sub>DD</sub> and V<sub>SS</sub> levels.

#### 6.4 $\overline{\text{RESET}}$ - Reset IC to Default State

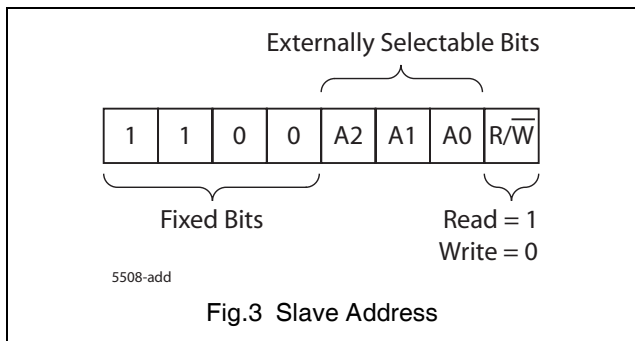
The active low  $\overline{\text{RESET}}$  input is used to disable the buffer, and reset it to its default state. The  $\overline{\text{RESET}}$  signal will clear the contents of the control register, turning off all output ports, and resetting the state of the I<sup>2</sup>C slave transceiver block.

#### 6.5 Power On Reset (POR)

During power-on, the IES5508 is internally held in the reset condition for a maximum of t<sub>RST</sub> = 500ns. The default condition after reset is for the Control Register to be Erased (all zeros), resulting in all output ports being off (high-impedance).

### 6.6 A0, A1, A2 - Address lines

The slave address of the IES5508 is shown in the Figure 3. The address pins (A2..0) must be driven to a HIGH or LOW level - they are not internally pulled to a default state.

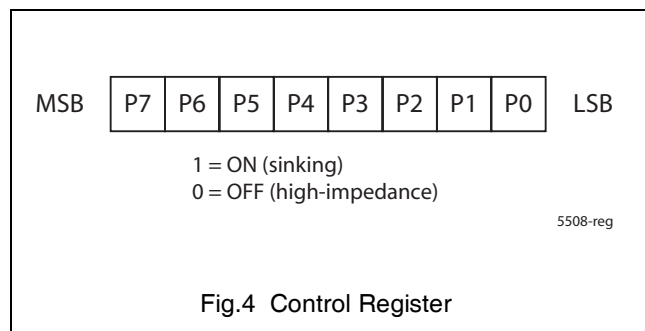


The read/write bit must be set LOW to enable a write to the control register, or HIGH to read from the control register.

### 6.7 Control Register

The control register of the IES5508 is shown in the Figure 4. Each of the output ports can be activated independently, by setting the appropriate bit in the control register.

A LOW or zero bit indicates that the respective channel (P7 to P0) is disabled (high-impedance). The default reset condition of the register is all zeros, all ports high-impedance. A HIGH or one bit indicates the respective channel is active (sinking).

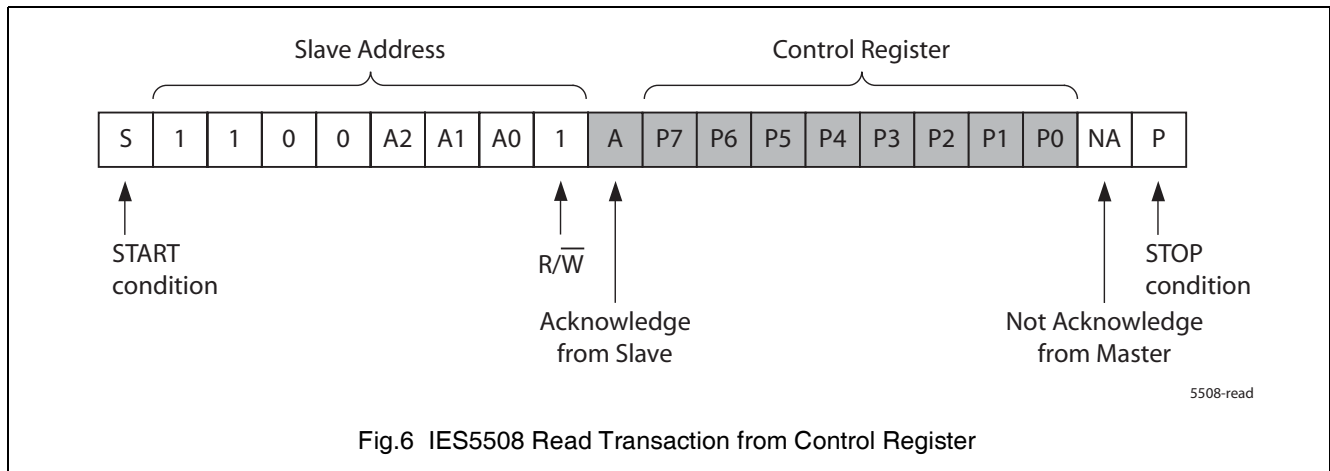
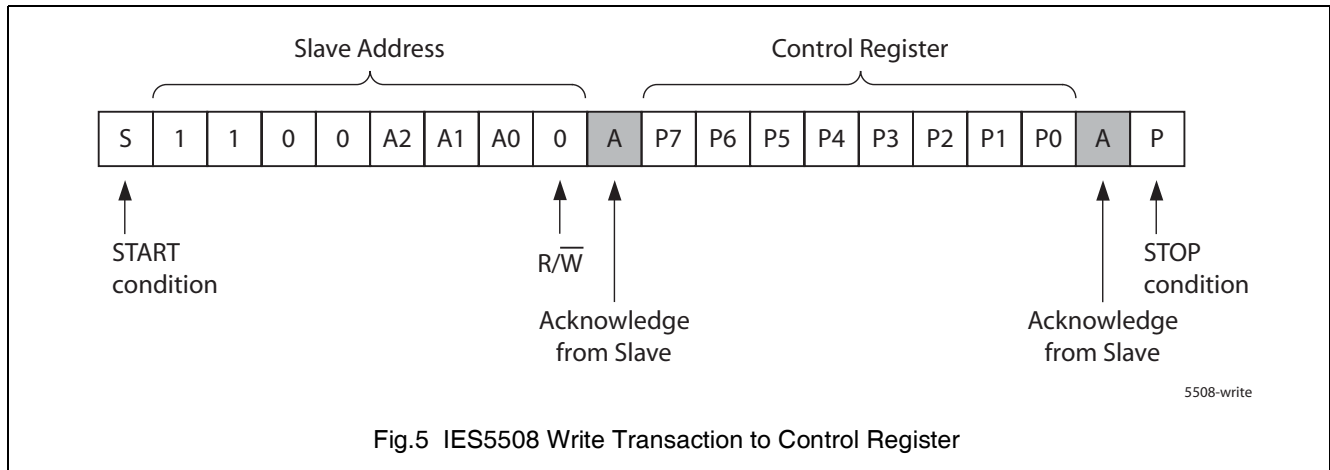


Example: Programming C1<sub>HEX</sub> (11000001<sub>BIN</sub>) into the control register results in ports P0, P6 and P7 being ON (sinking) and the remaining ports being OFF (high-impedance).

### 7 BUS TRANSACTION

A typical I<sup>2</sup>C write transaction to the IES5508 (slave) is shown in Figure 5. During a write transaction, the Output ports (P0 - P7) of the IES5508 are updated upon receipt of the STOP condition.

A typical read transaction is shown in figure 6.



### 8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134) Voltages are specified with respect to pin 8 ( $V_{SS}$ )

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DD}$	Supply voltage range ( $V_{DD}$ )		-0.3	+7	V
$V_{Pin}$	Voltage range (any pin)		$V_{SS}-0.5$	$V_{DD}+0.5$	V
I	DC current (output ports)	Note 1	-	100	mA
	DC current (SDA/SCL)		-	40	mA
	DC current (A2 - A0, $\overline{RESET}$ )		-	20	mA
	DC current ( $V_{SS}$ pin)		-	550	mA
$P_{tot}$	total power dissipation		-	300	mW
$T_{stg}$	storage temperature		-55	+125	°C
$T_{amb}$	operating ambient temperature		-40	+85	°C

#### Note

- 100mA for one pin only in the group P0 - P3, and one pin only in the group P4 - P7. Otherwise 70mA max, any pin.

### 9 CHARACTERISTICS

All specifications apply over the full operating temperature range of  $T_{amb} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ;

Voltages are specified with respect to pin 8 ( $V_{SS}$ );  $V_{DD} = 5.5\text{V}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	$V_{DD}(\text{V})$				
<b>Power supply</b>							
$V_{DD}$	supply voltage (operating)			2.7	-	5.5	V
$I_{DD}$	supply current (quiescent)	$V_{RST} = 0\text{V}$	5.5	-	-	0.1	$\mu\text{A}$
<b>I<sup>2</sup>C Ports (SCL / SDA)</b>							
$V_{Sxx}$	Bus voltage (SDX, SCX)			$V_{SS}-0.3$	-	$V_{DD}+0.3$	V
$V_{IL}$	LOW-level input voltage	[2]	2.7	-	-	0.4	V
			5.5	-	-	0.5	V
$V_{IH}$	HIGH-level input voltage	[2]	2.7	1.2	-	-	V
			5.5	2.0	-	-	V
$V_{HYS(Sxx)}$	Input Hysteresis	[2]	2.7	80	-	-	mV
			5.5	200	-	-	mV
$I_{IL}$	Input low leakage current	$V_{Sxx} = V_{DD}$		-	-	$\pm 0.1$	$\mu\text{A}$
$I_{OL}$	Output low sink current	$V_{Sxxin} < V_{IL}$		30	-	-	mA
$V_{OL}$	Output low voltage	$I_{OL} = 30\text{mA}$	2.7	-	260	450	mV
			5.5	-	140	275	mV
<b>Open Drain Output Ports (P0 to P7)</b>							
$I_{P7..0}$	Output low sink current	Port enabled		65	-	-	mA
$V_{P7..0}$	Output low voltage	$I_{OL} = 65\text{mA}$		-	440	725	mV
		$I_{OL} = 100\mu\text{A}$		-	1	-	mV

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>DD</sub> (V)				
<b>RESET</b>							
V <sub>RST(hi)</sub>	HIGH-level input voltage		2.7	2.0	–	–	V
			5.5	4.8	–	–	V
V <sub>RST(lo)</sub>	LOW-level input voltage		2.7	–	–	650	mV
			5.5	–	–	900	mV
V <sub>RST(hys)</sub>	RESET Hysteresis		2.7	100	–	–	mV
			5.5	200	–	–	mV
I <sub>RST</sub>	Input leakage current	V <sub>RST</sub> = V <sub>DD</sub>	–	–	±0.1	–	μA
t <sub>w-RST(lo)</sub>	LOW-level reset time	V <sub>RST</sub> < V <sub>IL(RST)</sub> [1]	–	25	–	–	ns
t <sub>RST</sub>	Reset (and POR) time	from V <sub>RST</sub> > V <sub>IH(RST)</sub>	–	250	500	–	ns
<b>Address A0, A1, A2</b>							
V <sub>A2..0(hi)</sub>	HIGH-level input voltage		2.7	1.7	–	–	V
			5.5	3.5	–	–	V
V <sub>A2..0(lo)</sub>	LOW-level input voltage		2.7	–	–	0.7	V
			5.5	–	–	1.5	V
I <sub>A2..0</sub>	Input leakage current	V <sub>A2..0</sub> = V <sub>DD</sub>	–	–	±0.1	–	μA
<b>Timing Characteristics</b>							
t <sub>f</sub>	SDA port Fall Time (ACK)	R <sub>Sxx(PULLUP)</sub> = 200ohm	–	16	–	–	ns
t <sub>p</sub>	Time between STOP condition and Output Port (P0 to P7) being asserted		–	–	500	–	ns

### Notes

- [1] Guaranteed by design, not subject to test.
- [2] Supply voltage dependant. Refer graphs for typical trend.
- [3] R<sub>Sxx(PULLUP)</sub> = 200ohm. SDA port fall time measured from 70% V<sub>DD</sub> to 30% V<sub>DD</sub>.

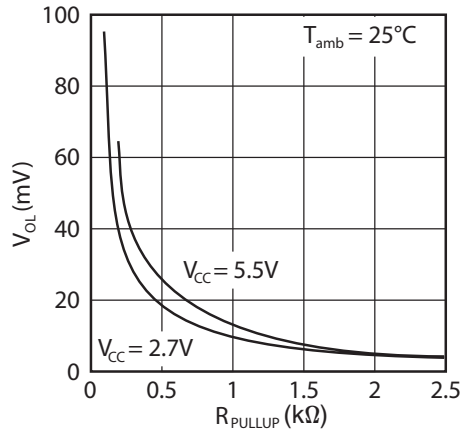


Fig.7 Typical SDA  $V_{OL}$  vs. pull-up resistance

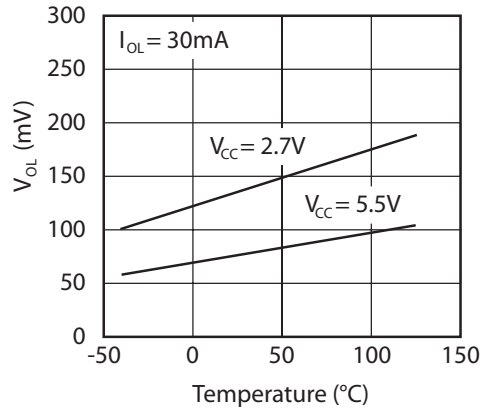


Fig.8 Typical SDA  $V_{OL}$  vs. Temperature

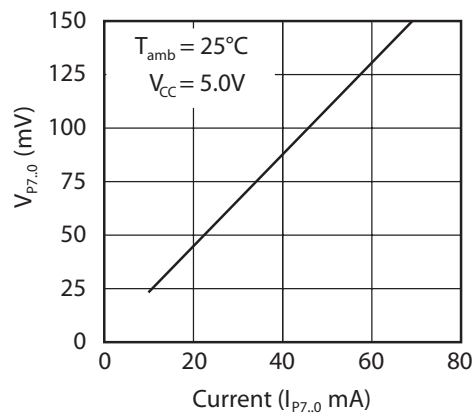


Fig.9 Typical Output Port Voltage ( $V_{P7..0}$ ) vs. Current ( $I_{P7..0}$ )

### 10 APPLICATION INFORMATION

#### 10.1 Design Considerations

Figure 10 shows the IES5508 in conjunction with the IES5507 bus multiplexer in a LED drive application. Each IES5508 can drive 8 LEDs, and using the address pins on the IC, up to 8 uniquely addressed devices can sit on one bus branch. The IES5507 has four such outputs, giving 256 LEDs in the structure shown.

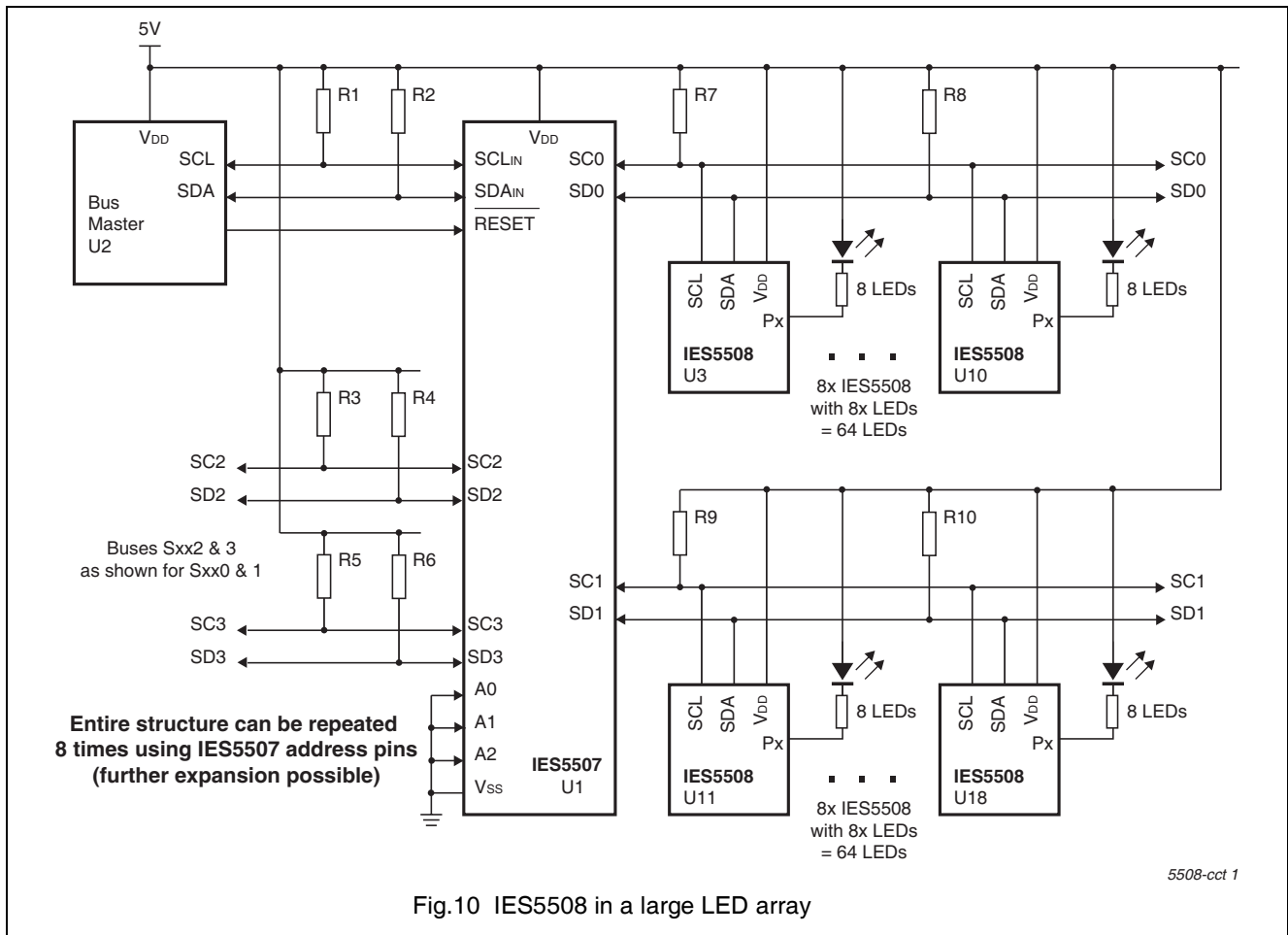
By additionally using the address pins on the IES5507, the entire structure may be repeated 8 times, allowing 2048 LEDs to be uniquely driven. By additionally placing IES5507's in series (refer IES5507 datasheet), the structure may be further extensively multiplied into a huge array.

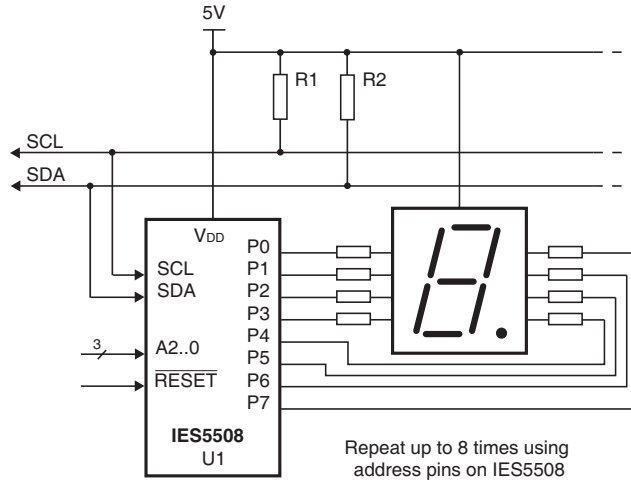
Figure 11 shows a simple 7-segment display drive arrangement. All of the 7-segments plus decimal point can be driven from a single IES5508. By using the address pins, up to 8 digits can be addressed from a single bus. When running at 1MHz, all 8 digits can be updated in less than 0.2ms.

Further, by using the arrangement described above and shown in Figure 10, the number of digits driven may be increased significantly.

Figure 12 shows the IES5508 used in conjunction with other Hendon Semiconductors 2-wire bus buffers to form a multiplexer arrangement. Using the IES5501 gives a bus multiplexer arrangement with full I<sup>2</sup>C compliant levels, low offset voltage and large noise margins. Using the IES5502 additionally gives "hot-insert" capabilities.

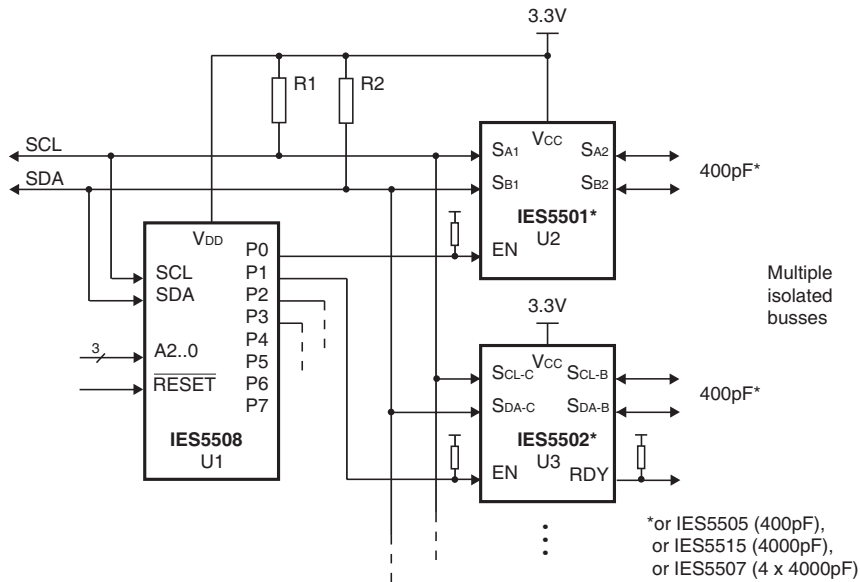
#### 10.2 Application circuits





5508-act2


Fig.11 IES5508 as 7-segment display driver



5501-act6

Fig.12 IES5508 as part of a fully isolating I<sup>2</sup>C-bus multiplexer (address lines allow this structure to be repeated 8 more times)

### 11 ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	NAME	DESCRIPTION	VERSION	ROHS
IES5508 T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT162-1	Yes 

Other package options are available - contact Hendon Semiconductors for details. For more information on packages, please refer to the document "Integrated Circuit Packaging and Soldering Information" on the Hendon Semiconductors web site.

### 12 ESD CAUTION

Electrostatic Discharge (ESD) sensitive device. ESD can cause permanent damage or degradation in the performance of this device. This device contains ESD protection structures aimed at minimising the impact of ESD. However, it is the users responsibility to ensure that proper ESD precautions are observed during the handling, placement and operation of this device.



### 13 DOCUMENT HISTORY

REVISION	DATE	DESCRIPTION
0.1	20080323	Draft objective specification
0.2		
0.3	20090305	Preliminary Specification
0.4	20090729	Modify Vol on ports in Characteristics Table
1.0	20091104	Product Specification & fix typo in general description

### 14 DEFINITIONS

<b>Data sheet status</b>	
Engineering sample information	This contains draft information describing an engineering sample provided to demonstrate possible function and feasibility. Engineering samples have no guarantee that they will perform as described in all details.
Objective specification	This data sheet contains target or goal specifications for product development. Engineering samples have no guarantee that they will function as described in all details.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later. Products to this data may not yet have been fully tested, and their performance fully documented.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

### 15 COMPANY INFORMATION

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