

I²C terminology explained

(TR000 V24.07.2008)



1. Basic Terminology

TERMINOLOGY	DEFINITION / DESCRIPTION	HOW, WHEN, AND WHERE IT'S RELEVANT
I ² C- bus	A serial bus communication system defined by a set of specifications. "Bus" simply means the wire, or wires, that link several connected devices enabling exchange of data via those wires.	It is a universally recognized bus defined by set specifications that ensure the correct inter-operation of components from many different manufacturers. It is a multi-drop bus capable of multi-master operation.
Standard-mode (Sm)	The original 100 kHz I ² C specification	
Fast-mode (Fm)	A revision to the I ² C specification in 1992 to 400 kHz with other improvements.	The I ² C specification updated in 1992 suggests that all devices from this date should, as far as possible, adopt the improvements (if not the full speed) that were added. Significant changes included hysteresis on inputs and a requirement to release the bus when a device is un-powered.
High-speed (Hs) Mode	An addition to the I ² C specification in 1998	Allowed 3.4 MHz speed, but essentially no devices support it.
Fast-mode Plus (Fm+)	Revision of the I ² C specification in 2007 to allow 1 MHz and 30 mA device sink capability.	Some software enhancements are also included.
Multi-drop bus	A bus that allows the connection of many devices, essentially in a parallel configuration, to a single set of signal (i.e. bus) wires.	It contrasts with 'point to point' buses that only allow the connection of, and transfer of data between, two devices
Master	The device that initiates communication, generates the SCL signal, and terminates the communication.	<p>Only a Master device can initiate communication with another device on the bus because it must provide the clock signal, set the basic timing of the data transfer, and provide the identification (address) of the device it will communicate with. The Master can be either the transmitter of data to a Slave device (or perhaps devices*) or the receiver of data from a (usually single) Slave device. It specifies the direction of the following data byte transfer by the 8th bit of the address byte. "1" or high for receive, "0" or low for transmit.</p> <p>(*It is usually an exception, but a Master can initiate simultaneous addressing and sending of data to multiple slaves on a bus).</p>
Multi-Master	A bus system that allows the role of the Master to be time-shared.	It allows any one of several Masters, situated anywhere on an I ² C- bus, to communicate with the other devices on the bus. There is a protocol to resolve the conflict over which one takes control should more than one Master attempt to take control at the same time.

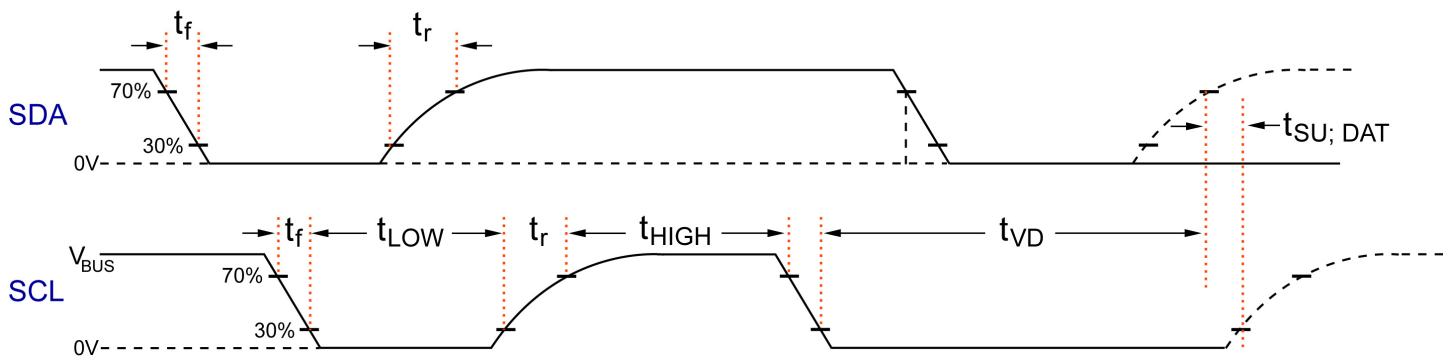
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Slave	Devices that are clocked/controlled by SCL timing signals and addressing generated by the Master	Slave devices can be either receivers or transmitters of data in the data exchange with the Master but the Master alone will determine the direction of the data flow.
Pull-up resistors	Resistors fitted between the bus lines and V_{BUS} to pull the bus lines towards the logic high voltage level.	Connected devices are only allowed to drive the bus to ground, causing a logic LOW level. While any one device is pulling the bus LOW the bus remains LOW. No device is allowed to drive the bus to logic HIGH level, only these pull-up resistors do that. Since ALL devices must be allowing a high level on the bus, in order to have the bus at a logic high, the I ² C logic configuration is sometimes referred to as a 'wired AND' configuration.
Bus capacitance	The total capacitance of each separate bus wire (either SCL or SDA) together with the total capacitance of the devices connected to it.	<p>This capacitance, together with the bus pull-up resistor, determines the bus exponential rise rate and so controls the bus rise time that has requirements that should be met. Even if those rise times can be met, the original Standard and Fast-mode specifications set an absolute bus capacitance limit of 400 pF. For Fm+ it is 550 pF. A note added to the I²C specification (dated 2007) suggests that if the appropriate rise time requirements are met it can be allowable to exceed the absolute bus capacitance limits.</p> <p>For example using a buffer or Fm+ driver, with 30 mA sink capability, allows the Fm bus rise time to be met on a 3.3 V bus having a total loading of 3650 pF. That bus will not strictly conform to any one I²C category, it is a mix of various classes, but it can be a valid application of I²C principles and operate just as reliably as any I²C class whose remaining specifications it does meet.</p>
Start	A unique pattern on SCL/SDA generated by a Master to indicate the start of a communication	The Master drives the SDA line low (from the idle state with both lines high) while the SCL is high. Note this is a special exception to the rule that SDA must not change while SCL is high.
Stop	A unique pattern on SCL/SDA generated by a Master to indicate the end of a communication	The Master releases the SDA line from a low level while the SCL line is high. The bus then becomes idle. Note this is a special exception to the rule that SDA must not change while SCL is high.
Acknowledge (ACK)	A data bit that concludes each address or data byte during communication.	<p>Provided on the SDA line during the Master's 9th clock cycle by the device that has received an address or data byte. A 'low' bit represents acknowledgement. It does not include any check that the data bits were correct, just that 8 bits were clocked in and the receiving device is ready to accept another byte. In the case of an address byte, an ACK (ie LOW) from a Slave indicates that the address as received matches its slave address and is available to communicate.</p> <p>Not ACK or NACK is used by an intended Slave receiver to indicate it is NOT ready to accept data, or by a Master receiver to indicate reception of the last data byte for the current transfer and that it does not require more data bytes from a slave.</p>

2. Voltage Parameters

VOLTAGE PARAMETERS	DEFINITION / DESCRIPTION	HOW, WHEN, AND WHERE IT'S RELEVANT
Bus supply voltage (V_{BUS})	The voltage to which the bus lines are connected via the bus pull-up resistors in an I ² C- bus system and the basis for all associated voltage specifications. In the I ² C specification it is written as V_{DD} because that is commonly used to designate the positive supply for CMOS devices that usually drive the bus.	Normally devices connected to the bus will have their supply voltage equal to the bus supply voltage so that their logic switching levels can meet the requirements. Since some devices are built using fast, but low voltage, IC processes their V_{CC}/V_{DD} may need to be set lower than V_{BUS} . In such cases care needs to be taken to remember that the logic switching levels of such devices is probably related to their supply, and not V_{BUS} , so their levels may not be I ² C- bus compliant.
Bus logic signal levels	The typical or limit value (or values) for the voltage on the bus at which a connected device must interpret the bus as being at either a logic LOW to a logic HIGH level.	Devices that are attempting to set the bus to a HIGH or LOW logic state must ensure these voltage levels on the bus are met so that each logic data bit they send will be correctly interpreted by the receiving device or devices. Devices receiving these levels must use logic switching levels that will correctly interpret these levels.
$V_{IL} = V_{input\ low}$.	The logic switching level of a device. The voltage level, referenced to ground, below which a chip receiving data from the bus interprets the bus as having a logic LOW level.	The I ² C- bus specification define this as any level below $0.3V_{BUS}$ but devices that include hysteresis require a different level. Many devices connected to the bus could have different, non-compliant, switching levels. For example the TTL levels used by SMBus and other derivative buses are not I ² C compliant. Some classes of buffers also use special non-compliant switching levels.
$V_{IL\ max.} = V_{input\ low\ maximum}$	The maximum voltage on the bus, referenced to ground, that an I ² C chip must always recognize as a valid bus logic LOW level. It is set at $0.3V_{BUS}$.	<p>When the bus voltage exceeds this value a receiving device may interpret the bus as being at a logic HIGH level. Devices driving the bus are therefore required to hold the bus lower than this value by a safety (noise) margin specified as $0.1V_{BUS}$ minimum. Standard-mode operation therefore requires the device driving the bus low to hold the bus below $0.2V_{BUS}$. Since Fm and Fm+ devices must have hysteresis the interpretation becomes more complex because such devices have two different switching thresholds, one for rising bus voltages and one for falling bus voltages. The Fm bus must be held below $0.25V_{BUS}$ and the switching threshold of its drivers, for a rising bus, must be above $0.35V_{BUS}$. See <i>noise margin</i>.</p> <p>If the driving device attempting to hold the bus at the logic LOW level fails to meet this requirement, as seen at one of the other connected devices, then there can be data or clocking errors causing bus system failures.</p>
$V_{OL} = V_{output\ low}$.	The voltage level required at the output of the device driving the bus LOW.	It is the voltage LOW level the bus driver device must produce, but not necessarily the voltage that it will cause to appear on the bus. The bus may be indirectly driven low, for example via series protection resistors or a bus buffer. The bus LOW requirement is derived indirectly from the V_{IL} , V_{HYS} , and noise margin specs.

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$V_{OL\ max} = V_{output\ low\ maximum}$	The maximum voltage at its output, referenced to ground, that the device is capable of holding while sinking an associated current level. The usual current used to define the maximum low level is either 3 mA for Standard and Fast-mode parts or 30 mA for Fm+ and some buffers.	This specified/guaranteed level, quoted at a particular current that the device is designed to sink, needs to be lower than the $V_{IL\ max}$ requirement of the bus and of all other devices on the bus. If it was not then those other chips could wrongly interpret the bus as being HIGH when it is intended to be LOW. To provide system design flexibility the specifications maintain a significant difference between V_{OL} and V_{IL} .
Noise Margin	The safety margin between the bus voltage and the bus voltage at which connected devices may interpret the logic level to be other than intended. For example the Noise Margin 'low', during a bus logic LOW condition, is the difference between the actual LOW voltage on the bus and the lowest V_{IL} of connected devices.	It indicates the margin (voltage amplitude) available for noise or other forms of offset or interference on the bus that can be tolerated without any corruption of the data or clock signals. It is therefore a measure of the reliability of signal transmission. The I ² C specification requires a minimum Noise Margin 'low' of $0.1V_{BUS}$ and Noise Margin 'high' of $0.2V_{BUS}$. These requirements, along with V_{IL} , V_{IH} requirements, are used to calculate the limits for the bus logic voltages and the driver device input switching thresholds.
Logic level shifting or logic level translation	The use of a buffer, or a FET or bipolar transistor in a common gate or common base configuration, to enable passing signals between one I ² C- bus and another I ² C- bus that has a different V_{BUS} .	<p>The interconnected buses usually share a common ground, ie bus logic low reference. Logic 'level shifting' then refers to an interfacing arrangement in which a LOW on either bus can pull the other bus LOW but each of the connected buses will be pulled up to a different bus supply voltage and have a different logic HIGH level.</p> <p>Simple common gate converters, including integrated versions, do not actually change the bus logic switching voltage levels to match the different switching levels used by each different bus, or provide any isolation of the bus loadings on the two connected buses. The I²C devices connected on either side of these simple devices must sink the sum of the pull-up currents in the pull-up resistors on each side of the device. They must also meet the logic switching level requirements of the devices on the lower voltage bus and both bus sections will have the (lower) noise margin that applies to the bus section having the lower V_{BUS}.</p> <p>Additionally the level shifting device has an offset (the LOW level on the driving side is slightly lower than on the driven side) and the device may impose additional restrictions on the driving side LOW level that may also affect noise margins.</p> <p>While a more complex buffer, with multiple supply voltages, might be able to provide I/O switching voltage levels adapted to the buses on each side, and loading isolation, they will generally be found to have other application constraints.</p>

3. Timing Parameters



TIMING PARAMETERS	DEFINITION / DESCRIPTION	HOW, WHEN, AND WHERE IT'S RELEVANT
Bus rise time (t_r)	The time taken for a bus line to transition from the guaranteed logic LOW level to the guaranteed logic HIGH level, i.e. from $30\%V_{BUS}$ to $70\%V_{BUS}$	The rise of the bus is a simple exponential rise, determined by the bus pull-up resistor and the capacitance on the bus line. Note carefully that the I ² C defined rise time is not the conventional logic one measured between 10% and 90% of the bus voltage that is often quoted for switching logic that uses active drive to both HIGH and LOW levels. The conventionally defined exponential rise time, the RC product (obtained by multiplying the pull-up resistor by the bus load capacitance) is the time to rise from 0V to 63% V_{BUS} . Thus the I ² C defined rise time is 0.85RC and the 10- 90% logic rise time is 2.2RC. The limits (maximum) for rise time are 1 μ s for Standard-mode, 300 ns for Fm, and 120 ns for Fm+
Bus fall time (t_f)	The time taken for a bus line to transition from the guaranteed logic HIGH level to the guaranteed logic LOW level, i.e. from $70\%V_{BUS}$ to $30\%V_{BUS}$	Because the bus is actively driven during falling edges the rate of fall is determined mostly by the characteristics of the device driving the bus. Generally the bus fall times will be approximately linear and much shorter than the exponential bus rise times. The limits (maximum) for fall time are 300ns for Standard and Fast-mode and 120 ns for Fm+. (Fm also has a minimum.)
Bus clock HIGH period	The time for which the bus clock line (SCL) is above the guaranteed bus logic HIGH level ($70\%V_{BUS}$)	The minimum limits for the bus HIGH period are 4 μ s for the Standard-mode, 600 ns for Fm, and 260 ns for Fm+. Note that these are all shorter than the corresponding requirements for the bus LOW period. When components that cause delays (buffers, cables) are added to a system the bus LOW period may need to increase, but the HIGH period does not. In order to have the fastest data clock frequency it is necessary to program different HIGH and LOW periods for the clock (SCL). When the master does not have the capability to provide different Hi/Lo periods then the HIGH period must be made equal to the (longer) LOW period and then the system runs significantly slower. Note it is the responsibility of the master to control this time period as it actually appears on the bus i.e. that master must also monitor the bus and should take into account the actual bus rise/fall times. I ² C has no maximum HIGH requirement but its variants mostly do.

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Bus clock LOW period	The time for which the bus clock line (SCL) is below the guaranteed bus logic LOW level (30%V _{BUS})	<p>The minimum limits for the bus LOW period are 4.7us for the Sm, 1.3 μs for Fm, and 500 ns for Fm+. The LOW period is the only time when the data outputs (SDA) are allowed to change, so this is the time during which drivers will generate each new data bit and change the SDA bus state as required. When components that cause delays (buffers, cables) are added to a system the bus LOW period usually must increase.</p> <p>The minimum LOW period will become the longer of a) the specified minimum or b) the sum of [tVD + tSU + sum of added delays]. The added delays to be summed are 1) the delay of the SCL falling edge as it travels from the master to the slave and 2) the delay of the valid data bit on SDA as it travels from the slave back to the master.</p> <p>Note it is the responsibility of the master to control this time period as it actually appears on the bus i.e. that master must also monitor the bus and should take into account the actual bus rise/fall times.</p>
tVD Time to valid data	The time period, measured from when the SCL line goes LOW, for a device to place its next data bit on the SDA line. It includes any rise or fall time component of that SDA line.	The I ² C-bus uses a serial data transmission. One bit of data can be transferred during each cycle of SCL. The data bus (SDA) must not change its data level except when the clock (SCL) is LOW. Each falling edge of SCL is the signal that requests the next bit of data to be placed on SDA. That new data bit must have settled to its correct level, including the bus rise or fall time and with some safety margin (tSU), before the SCL goes HIGH again.
tSU;DAT Data set-up time	The time period, measured to the rising edge of the clock (SCL), for which the data on SDA must be valid, that is, stabilized at its correct logic value.	This safety margin must always be included when calculating the necessary LOW period for the clock in systems that include buffers, cables, or other components that cause transmission delays. The (minimum) requirements are 250 ns for the Standard, 100 ns for Fast-mode, and 50 ns for Fm+.
Buffer propagation delays	The delay of either the SCL or SDA signal as it passes through any buffer device.	<p>The total signal delay caused by a buffer has two components.</p> <ol style="list-style-type: none"> An internal delay measured between when the input signal reaches its logic switching level and when its output starts to change, The rise or fall time of its output from when it starts to change until it reaches its valid level (30% or 70%V_{BUS}). <p>Since the V_{IL} and V_{OL} of buffers may have special levels that are not the 30/70% defined levels, they may create longer or shorter effective bus rise or fall times than the expected ones.</p> <p>The signal delay components may also have different values for the rising and falling edges. Some buffers create long 'effective' propagation delays by slowing or delaying the rise of the bus voltage in the region below 1 V.</p>

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Wiring (cable) delays	The time taken for logic signals to travel from one end of a cable to the other.	<p>Several factors are involved.</p> <ol style="list-style-type: none"> the signal that is generated at the 'input' end of the cable, the speed of light/electricity along the cable, the distortion of the signal at the output of the cable as compared to the input. <p>Since practical bus wiring will use cables having a characteristic impedance (100 Ω is typical) that is usually much smaller than the pull-up resistors that can be used to terminate it, there will be 'reflections' of the signal energy at the ends of the cable. Energy will often be reflected and travel back and forwards along the cable several times before the voltages at each end stabilize near their final logic value. The time for the signal levels to stabilize can represent a significant effective signal delay time because it can be a multiple of the time required for a signal to simply traverse the cable once. Without any such reflection effects, the speed a signal travel along a cable is about 5 ns/meter.</p>
Clock stretching	Increasing the LOW period of the Master's clock signal by a slave device or a buffer	<p>In theory any device that has the capability to drive the clock line LOW by its SCL I/O interface can vary the time the SCL line is LOW (in practice it can only increase it.) The master device should time each successive bus HIGH or LOW period using the actual bus voltages that it senses on the SCL line.</p> <p>In practice almost no slave devices have a driver on their SCL I/O and clock stretching by slaves is quite rare. Buffers generally will have drive capability on both SCL and SDA lines and may affect (stretch) the SCL timing. The buffer causes what is described as bit-wise clock stretching because it increases the LOW period of every SCL (bit) clock cycle.</p> <p>The buffer's internal propagation delays cause the stretching because, after the Master releases the SCL line, a buffer will generally hold that line LOW during the time taken for the signal to travel to the slave side of the buffer, then to have the connected slave bus go HIGH, and for that slave bus HIGH level to travel back through the buffer to the master side again.</p> <p>When programming the minimum clock LOW period into the Master, a designer may take into account any increases (stretching) that will be caused by buffers.</p>

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