

Short summary of features	Unit	Sx side of P82B96	Tx/ Rx side of P82B96	Sx side of PCA9600	Tx/ Rx side of PCA9600	Sx side of P82B715	Lx side of P82B715	Hendon Semiconductors		
								Both sides IES5505	Both sides IES5515	Both sides IES5501/2
<b>Input switching levels characteristics</b>										
V <sub>IL</sub> Highest level that guarantees O/P LOW	V	0.6 <sup>1</sup>	0.42V <sub>CC</sub>	0.425 <sup>2</sup>	0.4V <sub>CC</sub>	— <sup>4</sup>	— <sup>4</sup>	0.6 <sup>1,3</sup>	0.6 <sup>1,3</sup>	0.3V <sub>CC</sub>
V <sub>IH</sub> Lowest level that guarantees O/P HIGH	V	0.7 <sup>1</sup>	0.58V <sub>CC</sub>	0.58 <sup>2</sup>	0.55V <sub>CC</sub>	— <sup>4</sup>	— <sup>4</sup>	1.9 <sup>1,3</sup>	1.9 <sup>1,3</sup>	0.41V <sub>CC</sub>
Compatible with 0.4 V I <sup>2</sup> C/TTL driver logic levels	-	✓	✓	✓	✓	✓	— <sup>6</sup>	✓	✓	✓
Meets Fast-mode LOW threshold > 0.35V <sub>CC</sub>	-	x	✓	x	✓	— <sup>4</sup>	— <sup>6</sup>	x	x	Typ
Compatible Fast-mode 0.25V <sub>CC</sub> max bus LOW	-	V <sub>BUS</sub> < 2.4V	✓	x	✓	✓	✓	x	x	✓
HIGH level meets I <sup>2</sup> C- bus noise margin specs	-	✓	✓	✓	✓	✓	✓ <sup>4</sup>	✓	✓	✓
<b>Output LOW drive level characteristics</b>										
V <sub>OL</sub> when sinking 3 mA (max)	V	0.88 <sup>1</sup>	0.4	0.74 <sup>2</sup>	0.4	— <sup>4</sup>	— <sup>4</sup>	0.3 <sup>2</sup>	0.3 <sup>2</sup>	— <sup>5</sup>
Max < Fast-mode noise margin 0.25V <sub>CC</sub> spec	-	V <sub>BUS</sub> > 3.5V	✓	V <sub>BUS</sub> > 3V	✓	— <sup>4</sup>	— <sup>4</sup>	✓	✓	✓
Compatible with I <sup>2</sup> C-bus V <sub>IL</sub> max level (0.3V <sub>CC</sub> )	-	V <sub>BUS</sub> > 2.9V	✓	✓	✓	✓ <sup>4</sup>	— <sup>6</sup>	✓	✓	✓
Compatible with TTL bus max LOW level (0.8 V)	-	I <sub>SINK</sub> < 0.2mA <sup>1</sup>	✓	✓	✓	✓ <sup>4</sup>	— <sup>6</sup>	✓	✓	✓
<b>Output driver sink capability</b>										
Minimum Standard 3 mA static sink capability	-	✓	✓	✓	✓	✓	— <sup>7</sup>	✓	✓	✓
Additional, enhanced, static sink capability	-							4 mA		4 mA
Enhanced 30 mA (Fm+) static sink capability	-	x	✓	x	✓	x	✓	x	✓	x
This output suitable for driving long cables	-	x	✓	x	✓	x	✓	x	✓	x
<b>Other I/O characteristics</b>										
Allowed to parallel several of these I/Os	-	x	✓	x	✓	✓	✓	✓	✓	✓
I/O sources current (>10 µA allowed by I <sup>2</sup> C spec)	-	No	No	Yes	No	Yes	Yes	No	No	No
Drive has load component due other I/O's load	-	No	No	No	No	Yes	Yes	No	No	No
Logic level shifting capability on this I/O	-	✓	✓	✓	✓	x	x	x	x	✓
Connected bus voltage may exceed V <sub>CC</sub>	-	✓	✓	✓	✓	x	x	x	x	✓
Noise during LOW on I/P is transferred to O/P	-	No	No	No	No	Yes	Yes	No	No	Yes

Short summary of features	Unit	Sx side of P82B96	Tx/Rx side of P82B96	Sx side of PCA9600	Tx/Rx side of PCA9600	Sx side of P82B715	Lx side of P82B715	Both sides IES5505	Both sides IES5515	Both sides IES5501/2
<b>I<sup>2</sup>C to/from unidirectional components</b>										
Split transmit and receive	-	—	✓	—	✓	—	—	—	—	—
Input (Rx) logic levels are I <sup>2</sup> C compliant	-	—	✓	—	✓	—	—	—	—	—
Output (Tx) drive is I <sup>2</sup> C compliant	-	—	✓	—	✓	—	—	—	—	—
<b>Bus speed</b>										
Data suggests maximum bus speed	Hz	400 k	400 k	1 M	1 M	100 k	100 k	>1 M	>1 M	>1 M
Approx. propagation delay, this I/P to O/P	ns	70	200	50	70	(250)	0	10	10	100
Can be useful to at least this bus speed	Hz	700 k	700 k	1 M	1 M	400 k	400 k	1 M	1 M	1 M

**Notes:**

1. At +25 °C
2. Over rated temperature range
3. At  $V_{CC} = 5\text{ V}$ ,  $V_{CC}$  dependent
4. P82B715 has no switching threshold, the output follows the input for any output between 0 V and  $V_{CC}$
5. The output level depends on the input drive level, tracking about 50 mV above it.
6. The Lx side voltages are compatible, but I<sup>2</sup>C/ TTL would not normally interface to this side.
7. There would be no point using this side to drive 3 mA.
8. When driven with  $V_{IL} = 0\text{ V}$ .
9. With suitable input. Output depends on input drive level when drive < 0.6  $V_{typ}$ .
10. Output will exceed 0.4 V for typical input drive levels.