

Noise Margin in I²C- bus systems

The noise margins in a bus logic system are a measure of its 'safety margins' regarding immunity to noise that may be coupled into the system wiring or voltage differences that may exist between different points in the system. There can be differences in the ground potential and tolerances on the supply voltages of the different devices connected to the bus etc.

It represents the difference between the actual logic voltage on the bus at a point where a device is connected and the voltage level that may cause the connected device to wrongly interpret that logic level.

Noise margin (LOW) measures the margin between the actual logic LOW voltage on the bus and the input logic switching threshold at which the device may (or will) interpret the bus as being at the HIGH logic level. The noise margin (HIGH) is the difference between the bus HIGH level and the switching threshold of a

connected device which may cause that level to be interpreted as a LOW.

The I²C- bus specifications define the logic switching levels for devices that connect to the bus, and the characteristics of the SDA/ SCL bus lines, as shown in these two extracts from the specifications (I²C- bus specification, Table 1 and 2).

Table 1 defines the maximum level for a bus LOW as 30%V_{DD}, and the minimum level for a bus HIGH as 70%V_{DD}, where V_{DD} means the voltage to which the bus is pulled by the bus pull-up resistors and is the nominal operating voltage of the bus.

LOW level input voltage, $V_{IL} = 0.3V_{DD}$ eqn. 1.

Table 1: Characteristics of the SDA and SCL I/O stages

PARAMETER	SYMBOL	Standard-mode		Fast-mode		Fast-mode Plus		UNIT
		Min.	Max.	Min.	Max.	Min.	Max.	
LOW level input voltage	V_{IL}	-0.5	$0.3V_{DD}$	-0.5	$0.3V_{DD}$	-0.5	$0.3V_{DD}$	V
HIGH level input voltage	V_{IH}	$0.7V_{DD}$	(1)	$0.7V_{DD}$	(1)	$0.7V_{DD}$	(1)	V
Hysteresis of Schmitt trigger inputs: $V_{DD} > 2\text{ V}$ $V_{DD} < 2\text{ V}$	V_{hys}	n/a	n/a	$0.05V_{DD}$	-	$0.05V_{DD}$	-	V
		n/a	n/a	$0.1V_{DD}$	-	$0.1V_{DD}$	-	V
LOW level output voltage (open drain or open collector) at 3 mA sink current: $V_{DD} > 2\text{ V}$ $V_{DD} < 2\text{ V}$	V_{OL1}	0	0.4	0	0.4	0	0.4	V
	V_{OL3}	n/a	n/a	0	$0.2V_{DD}$	0	$0.2V_{DD}$	V
LOW level output current at 0.4V V_{OL}	I_{OL}	3	n/a	3	n/a	20	n/a	mA
LOW level output current at 0.6V V_{OL} (2)	I_{OL}	n/a	n/a	6	-	n/a	n/a	mA

Notes:

- (1) Maximum $V_{IH} = V_{DDmax} + 0.5\text{ V}$.
- (2) In order to drive full bus load at 400 kHz, 6 mA I_{OL} is required at 0.6 V V_{OL} . Parts not meeting this specification can still function, but not at 400 kHz and 400 pF.

Table 2: Characteristics of the SDA and SCL bus lines for Standard, Fast, and Fm+ I²C– bus devices

PARAMETER	SYMBOL	Standard-mode		Fast-mode		Fast-mode Plus		UNIT
		Min.	Max.	Min.	Max.	Min.	Max.	
SCL clock frequency	f _{SCL}	0	100	0	400	0	1000	kHz
Noise margin at the LOW level for each connected device (including hysteresis)	V _{nL}	0.1V _{DD}	–	0.1V _{DD}	–	0.1V _{DD}	-	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V _{nH}	0.2V _{DD}	–	0.2V _{DD}	–	0.2V _{DD}	-	V

Since the V_{IL}/ V_{IH} are absolute limits that must be observed, device classes with mandatory hysteresis must be designed to have actual input switching levels that must be above the V_{IL} and below the V_{IH} by at least the specified amount of hysteresis. Those different switching levels then need to be taken into account when calculating the “bus line” voltage limits of a bus system from the mandatory minimum noise margin requirements as specified in Table 2.

Table 1 separates the Fast-mode (Fm) and Fast-mode Plus (Fm+) into voltages classes, those above and those below 2 V nominal bus voltage, setting a different hysteresis limit and additional/tighter V_{OL} requirement for <2 V bus drivers.

For V_{DD} >2V, Table 2 requires Fast Mode or Fm+ Mode device switching levels to be >0.35V_{DD} and <0.65V_{DD}.

Device switching threshold for rising bus, input with hysteresis

$$= V_{IL} + V_{hys} = 0.3V_{DD} + 0.05V_{DD} = 0.35V_{DD} \dots \dots \text{eqn. 2.}$$

For V_{DD} < 2 V the device switching levels become >0.4V_{DD} and <0.6V_{DD}.

These indirect specification limits come from the requirement on the designer to place, for example, the device’s switching level for a rising bus above 0.35V_{DD} to ensure that, after the effects of 0.05V_{DD} hysteresis, the device still guarantees to recognise the bus as low if it falls back to 0.3V_{DD}. If on rising to, say, 0.34V_{DD}

the device’s switching threshold had been crossed, and the 0.34V_{DD} accepted as a bus HIGH, then if the bus subsequently fell by the required minimum hysteresis of 0.05V_{DD} it would then be at the level 0.29V_{DD}. The 0.05V_{DD} hysteresis requirement means the driver device must not change its state again, yet the bus voltage is now below the ‘absolute’ V_{OL} requirement of 0.3V_{DD} and needs to be recognised as being LOW.

The hysteresis and V_{OL} requirements taken together can therefore only be met by placing the device’s switching threshold for a rising bus, above [V_{IL} + V_{hys} (min)]. Similarly, for a falling bus, it must be placed below [V_{IH} - V_{hys} (min)].

Devices may be connected to the bus lines via series spike suppression resistors so the V_{OL} (0.4 V max), as required of output driver stages, is not always the same as the voltage that actually appears on the bus lines when driven LOW.

Table 2 requires that the bus lines must be kept within limits that guarantee certain HIGH/LOW levels after allowing for the effects of those series resistors or leakage currents. They must be at least 0.1V_{DD} below the LOW switching level (0.35V_{DD}) and at least 0.2V_{DD} above the HIGH switching level (0.65V_{DD}).

That requires the bus lines to be held below a LOW level of $0.25V_{DD}$ and above a HIGH level of $0.85V_{DD}$ for a Fast-mode system with its hysteresis (or below $0.2V_{DD}$ and above $0.9V_{DD}$ for a Standard-mode system without hysteresis).

Bus LOW (max), with hysteresis and noise margin,
 $= V_{IL} + V_{hys} - V_{nL} = 0.3V_{DD} + 0.05V_{DD} - 0.1V_{DD}$
 $= 0.25V_{DD}$ eqn. 3

Table 1 requires devices driving the bus to output a fixed LOW level of 0.4V maximum (for $V_{DD} > 2V$) while Table 2 requires inputs to accept a V_{DD} -related bus LOW signal level up to at least $0.25V_{DD}$. The difference

($0.25V_{DD} - 0.4V$) is therefore the minimum that is always available to accommodate series spike suppression resistors and/or bus buffers having input-output voltage differences (offsets). The LOW levels specified for a Fast-mode or Fm+ bus system, and how they are related, are shown in Fig.1 and the HIGH levels are shown in Fig. 2.

The noise margins of an I²C- bus system calculated on the basis of these 'limit' specifications will be the "worst case" system noise margins and the typical margins can be significantly better because the device designer will attempt to centre the nominal switching levels between these specified limits

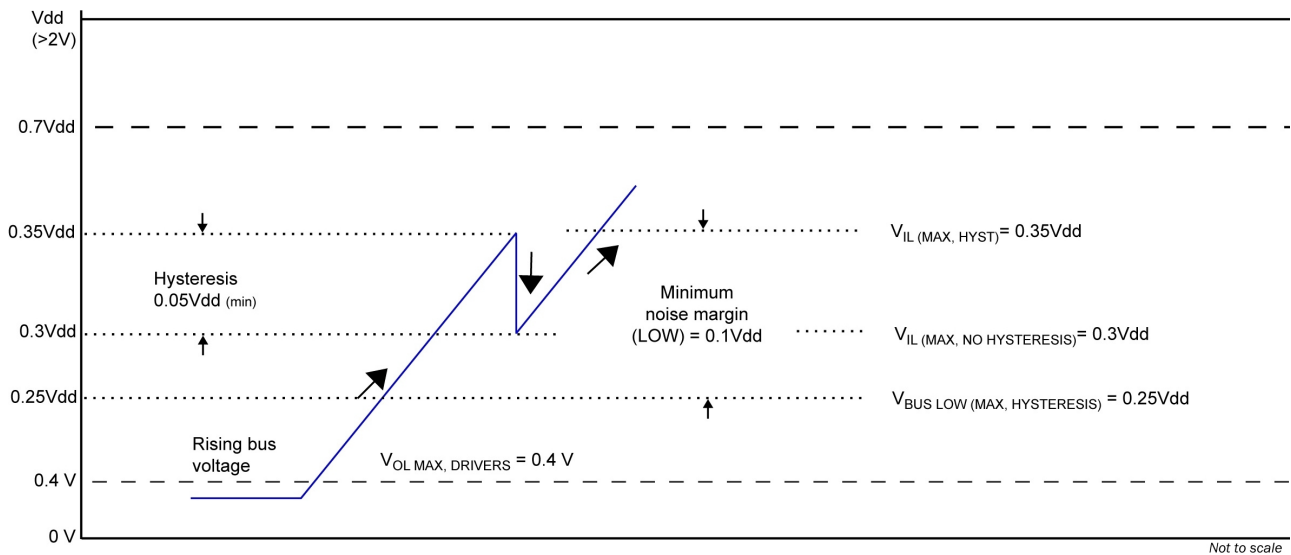


Figure 1: Specified bus LOW levels for Fast-mode or Fm+ that include mandatory hysteresis

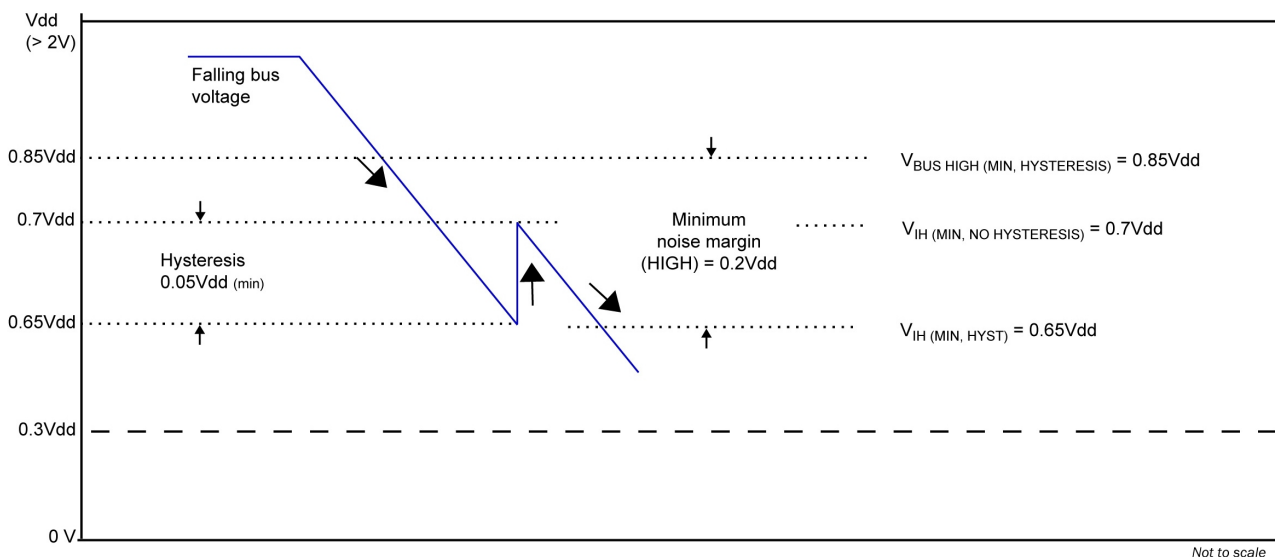


Figure 2: Specified bus HIGH levels for Fast-mode or Fm+ that include mandatory hysteresis

(For clarity in the examples in this document, as in the I²C- bus specifications, tolerances on the nominal bus voltage will not be included. Its tolerances should be included in the calculations when appropriate.)

Example 1: A typical simple system.

For a nominal 3.3 V bus system conforming to the Fast-mode requirements the specifications require the $V_{IL}+V_{hys}$ and $V_{IH}-V_{hys}$ switching thresholds of connected devices to be $0.35 \times 3.3 \text{ V} = 1.16 \text{ V}$ and $0.65 \times 3.3 \text{ V} = 2.15 \text{ V}$ respectively.

The Noise Margin specification in Table 2 requires that the bus lines be held below a level of $0.25 \times V_{DD} = 0.83 \text{ V}$ when it is low and above $0.85 \times 3.3 \text{ V} = 2.81 \text{ V}$ when high.

The I²C- bus devices driving the bus are required to drive a LOW level of 0.4 V, while the I²C- bus LOW requirement calculated from Tables 1 and 2 is 0.83 V. The difference (0.43 V in this case) is therefore available to accommodate series spike suppression resistors and/or bus buffers with input-output voltage differences (offsets).

For a 3.3 V system the mandatory minimum noise margin (LOW) of $0.1 V_{DD}$ represents just 330 mV, but notice that a typical design value for the switching threshold on a rising signal won't be the worst case $0.35 V_{DD}$, it is about $0.55 V_{DD}$ and on falling signals about $0.45 V_{DD}$. The typical noise margin for a system without series resistors, leakage, or buffers on a LOW is then above $(0.55 V_{DD} - 0.4 \text{ V}) = 1.42 \text{ V}$. And even that 0.4 V is the maximum allowed, the typical would be below 0.2 V, so the realistic noise margin is 1.62 V. That's nearly 5 times the worst case. On a HIGH it's typically $(V_{DD} - 0.45 V_{DD}) = 1.82 \text{ V}$. That difference between the typical and worst-case values is substantial and it is important that the system designer recognises and, as far as possible, works to preserve those full potential safety/noise margins as well as meeting mandatory minimums.

Example 2: Systems including devices powered from a supply that is lower than the I²C- bus voltage.

Many devices specified for operation on a V_{DD} supply 2.7 V – 3.6 V feature “5 V tolerant” I/Os that permit their operation on a nominal 5 V I²C- bus.

Including such parts, that generally won't meet the switching level requirements of a nominal 5 V Fast-mode I²C- bus, will affect the system noise margins. I²C- bus devices generally have switching thresholds related to their V_{DD} supply and, in this case, that is smaller than the bus voltage.

The worst-case switching thresholds calculated for the chip's nominal $3.3 V_{DD}$ remain the same as in example 1.

The 5 V bus requirements for the logic LOW signal to meet the noise margin spec requires the bus be held low below $(0.25 \times 5 \text{ V}) = 1.25 \text{ V}$. That will be met. The connected chips are required to recognise as a LOW any level up to $0.35 \times 5 \text{ V} = 1.75 \text{ V}$.

The “5V tolerant” devices, on their 3.3V supply, will have a TYPICAL switching level, for rising signals, at $0.55 V_{DD}$ or 1.82 V, so they typically will still meet this requirement. Worst-case, they are only required to recognise any level below $0.35 \times 3.3 \text{ V} = 1.16 \text{ V}$ as being LOW. That does not meet the 5 V bus requirement of 1.75 V.

Designing to meet worst-case tolerances would not allow the connection of “5 V tolerant”, but actually 3.3 V operational, devices to a 5 V bus. Typically there will be no problems, and the system will still have the guaranteed noise margin LOW of a 3.3 V system. The HIGH margins will be greater than the specification typical and worst case requirements. That gives the arrangement some practical advantage because bus lines when HIGH have much higher impedance, and less immunity to noise induced via capacitive coupling, than while driven, with a low impedance, to LOW.

Example 3: Systems including components specified for 'derivative' buses such as SMBus.

While the I²C- bus concept expects its components will usually have dedicated hardware interfaces with the specifications as above, most derivative buses have elected to use TTL logic levels instead of I²C logic levels because TTL interfaces are more available on the low cost general purpose microcontrollers they target for their application.

TTL interfaces, intended for fast logic signals, usually have no hysteresis and are not intended to work in noisy environments. TTL systems are not so precisely defined but they generally use the following levels. Driver V_{OL} is the same 0.4 V maximum and is defined with a sink current of at least the standard I²C- bus 3 mA level. (The SMBus Low Power requires only 350 μ A, but actual devices with that specification probably don't exist)

The bus LOW maximum requirement, V_{IL}, is specified at 0.8 V so the noise margin LOW is smaller than for I²C- bus.

The bus HIGH minimum requirement is a fixed 2.1 V rather than being a function of V_{DD}. Generally it will be easier to meet than the corresponding I²C- bus requirement. The values become equal for an I²C- bus voltage of 3 V.

Including those TTL parts in an I²C- bus system therefore has the following implications.

Their driver V_{OL} is the same so it does not affect the system.

For bus voltages above 2.7 V their worst-case V_{IL} requirement is tighter so they will have lower worst-case noise margins than the other I²C - bus components. In practice their actual switching threshold will be about 1.4 V so their typical noise margin LOW will be the same as a 3.3 V I²C- bus.

Including I²C - bus components in a TTL-based bus system has these implications. Their driver V_{OL} is the same so it does not affect the TTL system.

For bus voltages below 2.7 V the I²C- bus components have a tighter worst-case V_{IL} that would not be met by a TTL bus, but SMBus does not allow voltages below 2.7 V and other derivatives have even higher limits so in practice there are no additional requirements.

Designing an I²C system? Visit www.bus-buffer.com for more information or to contact us.