

## Non- isolating bus extenders

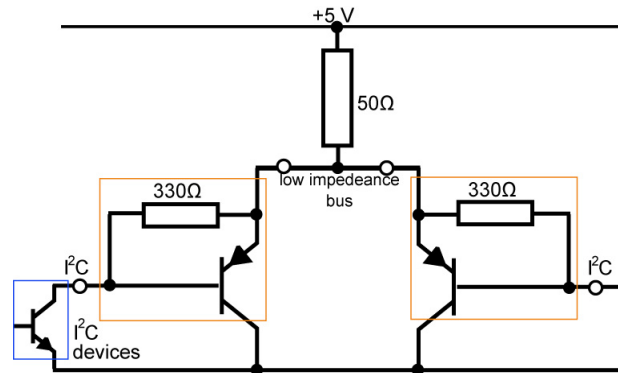


Figure 1: Simple impedance converter using an emitter follower

This device class is based on the earliest known attempts to extend the range of an I<sup>2</sup>C-bus using emitter followers to provide current amplification and increase the driver's sink capability. The current amplification is uni-directional, signals from the low impedance bus to the I<sup>2</sup>C-bus are not amplified, they simply pass via the 330 Ω resistor.

This simple emitter-follower approach as shown in Fig.1 sacrifices 0.7 V of valuable noise margin, because the drop across the transistor emitter-base means the low impedance bus line can only be pulled down to 0.7 V above the voltage at the I<sup>2</sup>C driver output, but it proved adequate in many applications.

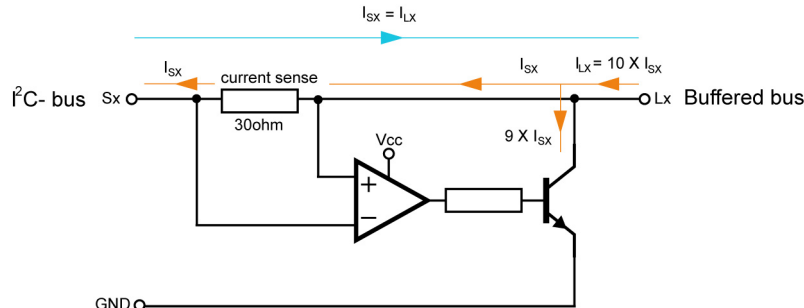


Figure 2: Simplified equivalent circuit of P82B715

The concept was refined, in the integrated circuit version P82B715, to the equivalent function shown in Fig. 2.

The action of this circuit is very similar in function to the simple emitter follower but has important differences.

- The current amplification factor can be controlled. It is set to a factor x10 so when the current sunk by the device at the Lx terminal is 30 mA that requires the I<sup>2</sup>C device connected at the Sx terminal to sink 3 mA.

- The voltage drop across the 30 Ω sense resistor is always less than 100 mV so it hardly affects noise margin and enables applications in lower voltage systems (e.g. 3.3 V) where the larger 0.7 V offset became significant.

At first the lower gain may appear a disadvantage because this arrangement now can't drive the 50 Ω bus in the first example. The bus load current at Lx would be  $(5\text{ V} - 0.7\text{ V}) / 50\ \Omega = 86\text{ mA}$  and that would require the I<sup>2</sup>C device to sink 8.6 mA.

The key advantage lies in the reverse situation, where the I<sup>2</sup>C-bus has a capacitance that must be charged

as the bus rises. When the buffer has a gain of x10 a capacitance of 100 pF on the I<sup>2</sup>C- bus at Sx becomes equivalent to an extra capacitance of 1000 pF to be charged up by the low impedance bus, and that slows its rise.

In the simple emitter follower version, where the transistor could have a gain of 200, the equivalent capacitance to be charged by the low impedance bus becomes 100 pF x 200 = 20 nF (and that means very slow rising edges).

Of course, if another pull-up resistor is always used on the I<sup>2</sup>C- bus (i.e. at the Sx terminal), it can cause the I<sup>2</sup>C- bus to attempt to rise faster than the low impedance bus then neither the emitter follower nor the P82B715 would be activated. (While not essential for operation of either circuit, it's "good practice" to fit pull-ups on both sides of these buffers.)

The P82B715 is not a symmetrical device, and it doesn't truly 'buffer' or isolate the loading on one I/O from the other.

When the Lx side of the device is pulled LOW the Sx side is simply pulled LOW via the internal 30 Ω resistor. None of the amplification circuitry is activated; the device is simply equivalent to a passive 30 Ω resistor. It creates no signal delays and the maximum static voltage drop across the 30 Ω resistor will occur if the Sx pin sinks the I<sup>2</sup>C maximum 3 mA.

The chip is specified to have a maximum static offset (Lx/Sx difference) of 100 mV and when driving lighter loads at Sx it is even smaller. Note that the device on the Lx side is carrying the I<sup>2</sup>C- bus current that is sunk at the Sx pin. The Sx and Lx currents are equal in magnitude as illustrated at the top of Fig. 2.

If the Sx side is pulled LOW, current flows from the Lx side in the current sense resistor. This activates the amplifier and causes a current, 9 times larger than the sensed current, to flow to ground in the transistor as shown. That means the total current flowing into the Lx terminal will be 10 times the current flowing out the Sx terminal. When an I<sup>2</sup>C device at Sx is sinking the allowed 3 mA the Lx current can be 30 mA.

During falling edges an I<sup>2</sup>C- bus with significant capacitive loading requires the I<sup>2</sup>C driver to sink a 'dynamic' current that is approximately double the usually quoted 3 mA 'static' sink current. The P82B715 will then also sink higher peak currents at Lx.

In this active mode there is some delay before the current flows in the transistor, and therefore some delay before 30 mA can flow. During this delay time the only current flowing into Lx can be the current flowing out Sx to the I<sup>2</sup>C device. That means that the Sx pin cannot be pulled LOW until the buffer 'assists' with the larger sink current. The delay is only around 250 ns but the important point to note is that the input voltage at Sx cannot go LOW before the output voltage at Lx goes LOW.

#### RULES:

- The input and output voltages of this type of buffer are always essentially equal.
- The buffer doesn't have separate 'input' and 'output' VOLTAGES, the two must always be nearly equal.
- The voltage difference never exceeds the product of the Sx current flowing times the 30 Ω sense resistance – and for practical purposes it will always be found to be less than 100 mV.
- The 'input' and 'output' CURRENTS can be different, but only when Sx has a voltage lower than Lx.
- When designing this type of buffer into an I<sup>2</sup>C system the designer must make allowance for its input-output offset voltage.

For simplicity, all bus voltage levels quoted in this note are those applying to a Fast-mode or Fm+ system with mandatory hysteresis and with a bus voltage above 2 V. For values applying to other I<sup>2</sup>C bus variants see [TR004, Noise margin in I<sup>2</sup>C systems](#)

Compliance with I<sup>2</sup>C- bus specifications of hysteresis and noise margin requires the I<sup>2</sup>C- bus lines of the system be correctly controlled (driven by the buffers) whenever the bus voltage is required to be LOW. For a bus voltage V<sub>CC</sub> that means whenever the bus lines

need to be at or below  $0.25V_{CC}$ , the maximum allowed for the bus LOW level.

P82B715 has a maximum offset of 100 mV so the system designer should ensure the buses at either side could be driven down to  $(0.25V_{CC} - 0.1 V)$ . For the usual system, that will use two P82B715s in series with their Lx sides linked and will therefore add two offsets, it means the I<sup>2</sup>C- buses connected at either Sx terminal need to be driven below  $(0.25V_{CC} - 0.2 V)$ .

For example, a 3.3 V bus system requires the designer to ensure the buses connected at either Sx can be pulled below  $(0.25 \times 3.3 V - 0.2) = 0.63 V$  to guarantee the LOW voltage level specification at the other Sx is met. Since all devices for driving an I<sup>2</sup>C- bus are required to drive their output LOW to 0.4 V max this requirement can be met, and there is even some margin left (0.23 V) for series transient suppression resistors or other buffers where those are required.

This style of 'buffer' should not strictly be called a buffer because it does not provide any isolation between the buses connected on its two sides. It is a uni-directional current amplifier, with bi-directional unity voltage gain, used as an impedance converter. The two buses that it connects are always linked by the 30  $\Omega$  resistor inside the chip. That is why there can be no isolation, and logic level shifting is not possible.

#### **Important characteristics of this type of buffer:**

- This device operates with a very low difference in voltage between its two I/Os making it compatible on its Sx side with virtually every I<sup>2</sup>C device and I<sup>2</sup>C buffer – including those buffers that use special logic switching levels on some I/Os.
- Just like all true I<sup>2</sup>C devices, there is no restriction on interconnecting multiple buffers together using either of their I/Os.
- The usual practical restriction on total capacitance applies and, uniquely for this part, calculations of that load capacitance must take account of 'transformed' loading – 1/10 of the loading at Lx appearing as loading at Sx.
- Since the I/Os are linked by a reasonably precise low value resistor, and available devices feature clamping diodes from the bus lines to  $V_{CC}$ , it is not

practical to include an 'enable' function in these extenders.

- Bus rise and fall times are slew limited, and quite slow, minimising potential for radiated EMI.
- P82B715 has clamp diodes fitted between each I/O pin and  $V_{CC}$ . While not allowed by the Fast-mode specification revision, they provide a practical solution to ESD protection of the I<sup>2</sup>C devices fitted at the Sx terminal when Lx is connected to long wiring or plugs/sockets etc. When designing for extreme levels of ESD these internal diodes can be shunted by larger diodes. Used in combination with a solid clamping of the  $V_{CC}$  supply this can provide the best practical ESD protection for the attached low voltage I<sup>2</sup>C parts.

#### **Where this part is most useful:**

- 1) Driving long wiring. With a buffer at each end of twisted pair cables, for example the pairs found in Cat5 Ethernet wiring, and when operating with a 5 V bus supply a cable length of at least 40 m can be used. The relatively slow bus rise and fall times produced by this buffer minimize ringing and overshoot on the cable signals.
- 2) When it is required to build a relatively short bus system, but with much more capacitance than the 400 pF specification, and where the bus logic LOW levels will not be compatible with the special logic levels required by other types of buffer. If it is correctly designed it is possible to have a total system capacitance of around 3000 pF running with bus voltages that are compatible with all I<sup>2</sup>C or derivative bus devices and with all other buffers. One example is its application in the IPMB used in AdvancedTCA systems where some other buffer types used in the system requires bus logic LOW levels to be below 0.4 V. With bus driving devices selected to achieve bus 'lows' well below the usual 0.4 V max requirement, P82B715s can allow a practical solution to be built. With its small input-output differential (or "offset") typically below 70 mV this buffer allows building radial systems that have a typical total capacitance around 2800 pF.

Designing an I<sup>2</sup>C system? Visit [www.bus-buffer.com](http://www.bus-buffer.com) for more information or to contact us.

Short summary of features	Unit	Sx side of P82B715	Lx side of P82B715
<b>Input switching level characteristics</b>			
V <sub>IL</sub> Highest level that guarantees O/P LOW	V	— <sup>1</sup>	— <sup>1</sup>
V <sub>IH</sub> Lowest level that guarantees O/P HIGH	V	— <sup>1</sup>	— <sup>1</sup>
Compatible with 0.4 V I <sup>2</sup> C/TTL driver logic levels	-	yes	— <sup>2</sup>
Meets Fast-mode LOW threshold > 0.35V <sub>cc</sub>	-	— <sup>1</sup>	— <sup>2</sup>
Compatible Fast-mode 0.25V <sub>cc</sub> max bus LOW	-	yes	yes
HIGH level meets I <sup>2</sup> C-bus noise margin specs	-	yes	yes <sup>1</sup>
<b>Output LOW drive level characteristics</b>			
V <sub>OL</sub> when sinking 3 mA (max. Volts)	V	— <sup>1</sup>	— <sup>1</sup>
Max < Fast-mode noise margin 0.25V <sub>cc</sub> spec	-	— <sup>1</sup>	— <sup>1</sup>
Compatible with I <sup>2</sup> C-bus V <sub>IL</sub> max level (0.3V <sub>cc</sub> )	-	yes <sup>1</sup>	— <sup>2</sup>
Compatible with TTL bus max LOW level (0.8 V)	-	yes <sup>1</sup>	— <sup>2</sup>
<b>Output driver sink capability</b>			
Minimum Standard 3 mA static sink capability	-	yes	— <sup>3</sup>
Additional, enhanced, static sink capability	-		
Enhanced 30 mA (Fm+) static sink capability	-	no	yes
This output suitable for driving long cables	-	no	yes
<b>Other I/O characteristics</b>			
Allowed to parallel several of these I/Os	-	yes	yes
I/O sources current (>10 uA allowed by I <sup>2</sup> C spec)	-	yes	yes
Drive has load component due other I/O's load	-	yes	yes
Logic level shifting capability on this I/O	-	no	no
Connected bus voltage may exceed V <sub>cc</sub>	-	no	no
Noise during LOW on I/P is transferred to O/P	-	yes	yes
<b>I<sup>2</sup>C to/from unidirectional components</b>			
Split transmit and receive	-	no	no
Input (Rx) logic levels are I <sup>2</sup> C compliant	-		
Output (Tx) drive is I <sup>2</sup> C compliant	-		
<b>Bus speeds</b>			
Suggested maximum bus speed	kHz	100	100
Approx. propagation delay, this I/P to O/P	ns	(250 ns)	0 ns
Can be useful to at least this bus speed	kHz	400	400

## Notes:

1. P82B715 has no switching threshold, the output follows the input for any output between 0 V and V<sub>cc</sub>. The voltage at Sx will not exceed the voltage at Lx by more than 0.1 V. If the input Lx level is designed to be below (0.25V<sub>cc</sub> – 0.1 V) then the Sx output will be I<sup>2</sup>C compliant.
2. The Lx side voltages are compatible, but I<sup>2</sup>C/TTL would not normally interface to this side.
3. Lx may be used to sink any current up to the maximum static 30 mA but there would be no advantage when using this output to sink 3 mA.