Isolating buffers using true voltage followers

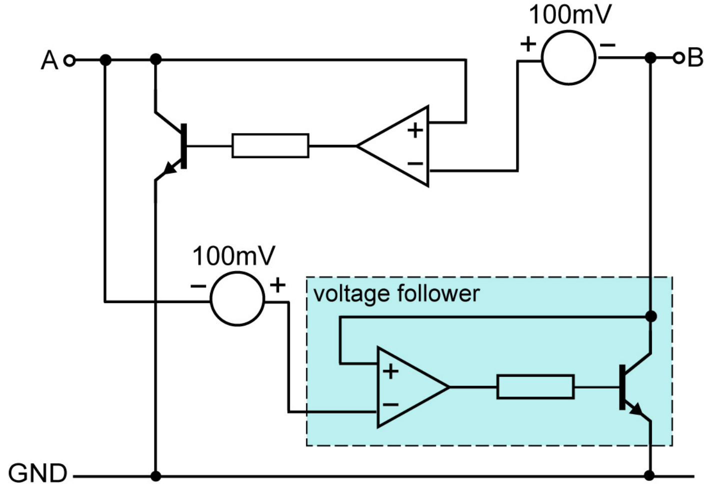

Figure 1: A true voltage follower circuit

This class of buffer also solves the latching problem explained in TR002 (Techniques for buffering I^2C signals) by ensuring that the voltage output from the buffer on either side is always slightly higher than the input voltage necessary to drive its other side LOW. The difference in this buffer is that the fixed 'special' logic levels of other buffers are replaced by a 'dynamic' level adjustment arrangement that simply makes its output slightly higher than the input. It uses voltage followers plus small dc offsets to achieve the non-latching requirement.

In this example, a voltage V that is input at 'A' will cause output 'B' to be driven down to (V+100 mV). That input level at 'B" will, in turn, only attempt to drive 'A' down to a level (V+ 100 mV + 100 mV) and, since 'A' is already down at the lower voltage V, that drive is inactive at the I/O and there can be no latching. By minimising the offset that is used (and typical values are as low as 25 mV) this arrangement has minimal impact on the I^2C- bus voltage levels and hardly affects the system's noise margins.

For simplicity, all bus voltage levels quoted in this note are those applying to a Fast-mode or Fm+ system with mandatory hysteresis and with a bus voltage above 2 V. For values applying to other I^2C- bus variants see TR004 (Noise margin in I^2C systems)

In the simplified Fig.1 it appears that the buffer will handle all input signal levels between 0 V and the buffer supply voltage but building a buffer with that (rail-to-rail) input voltage capability would be more complex/costly than is necessary.

Note that as the bus is falling from V_{CC} any bus voltage down to $0.65V_{CC}$ must be treated as logic HIGH, so in that range a buffer certainly has no need to be active. It is only at bus levels below $0.25V_{CC}$, the maximum allowed bus LOW level, that the buffer in a system must ensure that it correctly outputs the bus LOW signal level when fed with the necessary input level.

If this buffer is only enabled as the bus voltages approach their LOW level then this arrangement can be used to achieve logic level shifting while maintaining isolation of the bus (HIGH) noise components and loadings on its two opposite sides. Circuitry is therefore added to the simplified illustration in Fig.1 to 'enable' the follower action only when the chip has power and when the input signal on one or other input has fallen to a level somewhere in the range below $0.65V_{CC}$ and above $0.25V_{CC}$.

In theory a buffer could also be built with the offset in only one of the two directions but in practice they are usually symmetrical, as shown here.

This construction results in a true buffer with a high input impedance, just the negligible loading of the sensing op-amp, that provides isolation of any loading on its other side. It is simple to add an 'Enable' input to

control when the buffer will be active. That allows it to be applied in hot insertion applications requiring the interface to be disabled during the initial connection and until conditions are suitable for allowing bus signals to pass. It can allow these buffers to perform some bus switch/multiplexer functions.
The buffer can be arranged to comply with the I^2C- bus noise margin requirements by simply arranging that the buffer correctly controls its output LOW whenever that output voltage is below $0.25V_{CC}$.

To comply with the bus LOW requirement on the buffered side of the buffer, $0.25V_{CC}$, the system designer simply designs the buffer's input voltage to accommodate its offset. For a buffer with a guaranteed maximum offset of 60 mV the LOW at its input must be kept below ($0.25V_{CC}$ – 60 mV). For a bus voltage of 3.3 V this requires the buffer input to be kept below 0.77 V. With all bus driving devices required to output a LOW of 0.4 V maximum the requirement is easy to meet, and even some series (spike suppression) resistors could still be incorporated.

Since these buffers are typically symmetrical, the design requirement is to ensure both buses linked by this buffer have their LOW kept below ($0.25V_{CC}$ – Vbuffer offset). It means the noise margin LOW of the I^2C- bus system including a buffer of this construction is typically degraded by its typical offset - as little as 25 mV - and the HIGH margin need not be affected.

Contrast with a buffer such as PCA9517 that uses fixed levels on one side to avoid latching. It has a fixed V_{IL} requirement of 0.4 V max, so theoretically it degrades the worst case system noise margin LOW to zero for the bus connected to that special input. Of course every buffer technique involves compromise. Voltage follower style buffers simply transfer any noise during the bus LOW from one side directly to the other, while buffers with fixed switching levels such as PCA9517 will isolate any bus noise that does not exceed its relevant switching thresholds.

Important characteristics of this type of buffer:

- Provides isolation between the bus loadings applied at each I/O. That is, the resistive/capacitive loading of the bus on side has no influence on the input impedance at the other side. That means using one buffer can double the allowed system bus capacitance.
- As for any I^2C compliant devices there are no special requirements regarding the connection of these buffers in parallel so paralleling several devices permits a very large total system capacitance.
- Makes only minimal changes to the existing bus LOW signal levels (typ 25-50 mV increase of LOW level) and controls its output LOW over the full range of the specified bus LOW voltage, ie up to $25\%V_{CC}$ for Fast-mode systems requiring hysteresis and of course to $20\%V_{CC}$ for the original Standard-mode systems without hysteresis.
- These low offsets allow the $0.25V_{CC}$ bus LOW requirement to be met even when several buffers are connected in series.
- I^2C- bus compliant logic output levels. (V_{IL} even up to at least $30\%V_{CC}$ is recognised and handled correctly).
- Fast switching times, suitable for operation to at least 1 MHz, are achieved with negligible input drive requirement.
- Specified static sink capability above 3 mA (e.g. 4 mA for IES5501), and has the possibility to be adapted to stronger drive capability, e.g. 30 mA for Fm+, or independent bus activation levels on each side.
- I/Os have very high voltage compatibility/ tolerance, independent of V_{CC}, e.g. 15 V bus voltage is allowed.
- Bus voltage level translation is possible up to the max bus rating (e.g. 15 V for IES5501). Just note that the input switching voltage levels are related to V_{CC} and not necessarily to the bus voltage. For example a buffer on V_{CC} = 5 V has a typical activation threshold of 1.65 V which guarantees it can output I^2C compliant LOW levels for buses up to 6.6 V, but not for a 15 V bus. A 15 V bus would require 3.75 V for compliance, but the 1.65 V still provides 'compatibility' with the 15 V bus because its bus drivers must be capable of driving down to 0.4 V. When the 15 V bus is HIGH, having higher impedance that is more prone to noise, the 1.65 V

threshold means it actually has an enhanced noise margin HIGH. When the bus is driven LOW it has quite low impedance and reduced noise coupling. So a level-shifted 15 V bus, even with the noise margin LOW of a 5 V bus, can provide a good practical solution.

There is a somewhat related class of buffers that cannot be included in this class because their characteristics are very different. They might be described as a 'hybrid' of the voltage follower and special fixed level buffer classes but they still do not belong in either class. Typically they include rise time accelerators and they exhibit a voltage follower characteristic only for some limited range of input voltage levels. They exhibit a follower action on falling bus edges but after the input falls below about 0.5 V their characteristic changes. If the input is then released and it attempts to rise it will be firstly constrained by the buffer to a very slow rise rate and, when it reaches a fixed switching level, typ. 0.6 V, it changes to the output release characteristic of a buffer that uses special fixed logic thresholds. The description of the near-ideal characteristics or the applications of 'true' voltage follower buffers described in this note do NOT apply to those 'hybrid' buffers.

Where this part is most useful:

1. Where true buffering (load isolation) is required and I^2C- bus logic level compliance cannot be compromised. It can provide the lowest offsets and therefore the closest approach to perfect buffering when compliance with worst-case I^2C switching thresholds is a top priority.

2. Used in combination with I^2C- bus switches that are based on simple FET switches. Those switches provide no isolation of their input side from the total loading that might be required on their outputs, especially when more than one output bus is selected. They also require buffers that have minimal offsets because the switch on-resistance depends on the applied input voltage and is mostly specified only for bus LOW voltages of 0.4 V. See DI001 (Buffering I^2C switches using IES5501) and DI002 (Driving large distribution systems).

3. In combination with the P82B715 it provides one of the easiest solutions for driving I^2C signals at moderate voltages/speeds, say 5 V/ 100 kHz, over simple twisted pair cables at least 30 m long. For higher speeds it allows the combination to easily meet the Fast-mode rise times and bus release requirement while retaining the slower P82B715 cable rise/fall times for improved EMC. See AN102 (Simplifying extended I^2C systems) and DI002 (Driving large distribution systems).

4. In Radial IPMB systems for AdvancedTCA it achieves the lowest signal offsets. When interfacing between legacy buffer components it can achieve signal offsets that are within 15mV of the offsets found in a bused system. For new designs it offers the possibility to build systems with I^2C compliant bus logic voltage levels and greatly improved noise margins. See DI007 (Shelf Manager with compliant I^2C levels)

5. With 'hot swap' logic added (as in IES5502) it provides an ideal replacement in AdvancedTCA and similar systems for the non-compliant buffers commonly used in those systems. Such buffers have some of the characteristics of true emitter-follower buffers but also have the special fixed-level switching thresholds of other buffers. In practice it means they have a non-compliant bus LOW release characteristic. They release their output for input bus LOW voltages around 0.4 V to 0.6 V so, working with an IPMB LOW requirement of 0.4 V, provide little or no noise margin. IES5502 allows the intended IPMB system noise margins to actually be achieved. See AN101 (Discrete RRA and IES5501) and AN103 (IES5501 in AdvancedTCA applications)

Short summary of features	Units	Both sides IES5501/2
Input switching level characteristics		
V_{IL} Highest level that guarantees O/P LOW	V	0.3Vcc
V_{IH} Lowest level that guarantees O/P HIGH	V	0.41Vcc
Output LOW drive level characteristics		
Compatible with 0.4 V I^2C/TTL driver logic levels	-	yes
Meets Fast-mode LOW threshold > 0.35Vcc	-	typ
Compatible Fast-mode 0.25Vcc max bus LOW	-	yes
HIGH level meets I^2C-bus noise margin specs	-	yes
Output driver sink capability		
V_{OL} when sinking 3 mA (max. Volts)	V	— [1]
Max < Fast-mode noise margin 0.25Vcc spec	-	yes
Compatible with I^2C-bus V_{IL} max level (0.3Vcc)	-	yes
Compatible with TTL bus max LOW level (0.8 V)	-	yes
Output driver sink capability		
Minimum Standard 3 mA static sink capability	-	yes
Additional, enhanced, static sink capability	mA	4
Enhanced 30 mA (Fm+) static sink capability	-	no
This output suitable for driving long cables	-	no
Other I/O characteristics		
Allowed to parallel several of these I/Os	-	yes
I/O sources current (>10 uA allowed by I^2C spec)	-	no
Drive has load component due other I/O's load	-	no
Logic level shifting capability on this I/O	-	yes
Connected bus voltage may exceed Vcc	-	yes
Noise during LOW on I/P is transferred to O/P	-	yes
I^2C to/from unidirectional components		
Split transmit and receive	-	no
Input (Rx) logic levels are I^2C compliant	-	
Output (Tx) drive is I^2C compliant	-	
Bus speeds		
Suggested maximum bus speed	MHz	>1
Approx. propagation delay, this I/P to O/P	ns	100
Can be useful to at least this bus speed	MHz	1

Note 1: The output level depends on the input drive level, tracking about 50 mV above it.